TC03 TAPE COUPLER

(TS11 COMPATIBLE)

TECHNICAL MANUAL

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TC0351001 Rev A
September 1985

WARNING

This equipment generates, uses, and can radiate radio-frequency energy, and if not installed and used in accordance with the technical manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of Federal Communications Commission (FCC) Rules, which are designed to provide reasonable protection against such interference when operating in a commercial environment. Operation of this equipment in a residential area is likely to cause interference, in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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EMULEX PRODUCT WARRANTY

SUBSYSTEM WARRANTY: Emulex warrants all packaged subsystems and their major elements, including host adapters, to be free of defects in material and workmanship for a period of six (6) months following shipment to the customer. In the event of difficulty, the customer should return the questionable assembly to Emulex, freight prepaid. Emulex, at its option, will either repair or replace the unit following confirmation that it is covered by our warranty. Major assemblies are defined as power supply, disk drive, tape drive, and all associated controller circuit boards which make up the packaged subsystem.

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NOTE

All expressed and implied warranties concerning the subsystem portion of this warranty are considered null and void if the subsystem is operated in a partially disassembled state. The subsystem must be run with all covers and outer shells in place.

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Section 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

This manual provides information related to the capabilities, design, installation, and use of the TC03 Magnetic Tape Coupler manufactured by Emulex Corporation.

The manual contains eight sections and two appendices:

Section 1 **General Description.** This section contains an overview of the TC03 Magnetic Tape Coupler.

Section 2 **Specifications.** This section contains specification tables for the TC03.

Section 3 **Planning the Installation.** This section contains the information necessary to plan your installation.

Section 4 **Installation.** This section contains the information necessary to set up and physically install the TC03.

Section 5 **Troubleshooting.** This section describes preventive maintenance and fault isolation procedures for maintaining optimum performance of the TC03.

Section 6 **Coupler Registers and Programming.** This section describes the registers and command packets.

Section 7 **Functional Description.** This section describes TC03 architecture.

Section 8 **Interfaces.** This section describes the tape transport interface and LSI-11 bus interface.

Appendix A **Autoconfigure, Base and Vector Addresses.** This appendix explains use of the algorithms for assignment of floating addresses and floating interrupt vector addresses used with RSTS/E and RSX-11M devices.

Appendix B **PROM Removal and Replacement.** This appendix provides instructions for removing and replacing PROMs.

Appendix C **Drive Configurations.** Presents configuration instructions for supported tape drives.

1.1.1 RELATED DOCUMENTATION

The DEC manuals listed in this subsection may be ordered from the following address:

Digital Equipment Corporation
P.O. Box CS2008
Nashua, NH 03061

Title:	RSX-11M System Generation and Installation Guide
Publication Number:	AA-H625C-TC
Title:	RSX-11M-PLUS System Generation and Management Guide
Publication Number:	AA-H431A-TC
Title:	RT-11 Software Support Manual
Publication Number:	AA-H379B-TC
Title:	RSTS/E System Generation Manual
Publication Number:	AA-2669G-TC
Title:	MicroVMS User's Manual
Publication Number:	AA-Z209B-TE

The following DEC publication may also be useful to readers:

The DEC Dictionary: A Guide to Digital's Technical Terminology

Available from:

Digital Press
30 North Ave.
Burlington, MA 01803

1.1.2 DEFINITIONS OF TERMS

This manual uses standard DEC terminology wherever possible. For definitions, see the DEC Dictionary (referenced in subsection 1.1.1). In some cases, however, Emulex has adopted alternate conventions in order to avoid the use of potentially ambiguous terms. Possible exceptions to standard usage are defined in this subsection.

- As applied to tape transports, the terms **non-streaming, formatted,** and **start/stop** are used interchangeably in this document.
- The term **LSI-11 bus,** as used in this document, is synonymous with DEC's **Q-Bus.**

- The term **base address** represents the same concept as the commonly-used terms **LSI-11 bus address, CSR address,** and **device address.** Because the TC03 has no Control and Status Register per se, the expression "CSR address" is avoided in this document wherever possible. In DEC prompts (e.g., subsection 4.7.2), "CSR" refers to the TSSR (Status Register), which is located at the base address plus 2.

- The term **file mark,** as used in this manual, is synonymous with **tape mark.**

- The term **subsystem,** as applied to the TC03, refers to an individual emulation (the tape coupler plus one transport). As explained in subsection 1.2, the TC03 emulates four DEC TS11 subsystems.

1.2 SUBSYSTEM OVERVIEW

The TC03 is an intelligent, microprocessor-based tape coupler that is capable of connecting up to four tape transports to DEC computer systems that use the LSI-11 bus. The tape transports must have internal formatters that use the industry-standard Pertec interface.

When used with an appropriate formatter and tape transports, the TC03 performs a software transparent emulation of four DEC (Digital Equipment Corporation) TS11 Tape Subsystems. The TC03 is supported by all DEC operating systems that run on LSI-11 systems (not including MicroVMS). The TC03 also supports the bootstrap options of DEC's TK25 and TSV05 Tape Subsystems. The TC03 is compatible with the standard TSDRIVER software supplied in DEC operating systems.

The TC03 functions with both streaming and non-streaming tape transports with integral formatters. The operating mode is determined by means of switches on the operator control panel of the tape transport, as explained in Section 4 of this document. The TC03 is hardware compatible with non-streaming (formatted) nine-track tape transport systems that operate with any of the following formats:

- Non-Return to Zero Inverted (NRZI) format at 800 bits per inch (bpi)

- Phase Encoded (PE) format at 1600 or 3200 bpi

- Group Code Recording (GCR) format at 6250 bpi

- Dual density (NRZI/PE or PE/GCR)

- Tri-density (NRZI/PE/GCR)

Streaming tape transports operate with the following formats:

- PE
- GCR
- Dual density (PE/GCR)

System tape transports may operate at any of the industry standard tape speeds from 12.5 to 140 inches per second (ips). In non-streaming mode, typical tape speed is 25 ips; check the manufacturer's specification for the exact speed. In streaming mode, typical tape speed is 100 ips. The TC03 shifts from non-streaming to streaming mode automatically if enough data is available to support the higher throughput rate. The shift is software transparent.

Tape transports supported by the TC03 may have any combination of formats and tape speeds within the range defined above.

Figures 1-1 and 3-2 show two possible TC03 subsystem configurations.

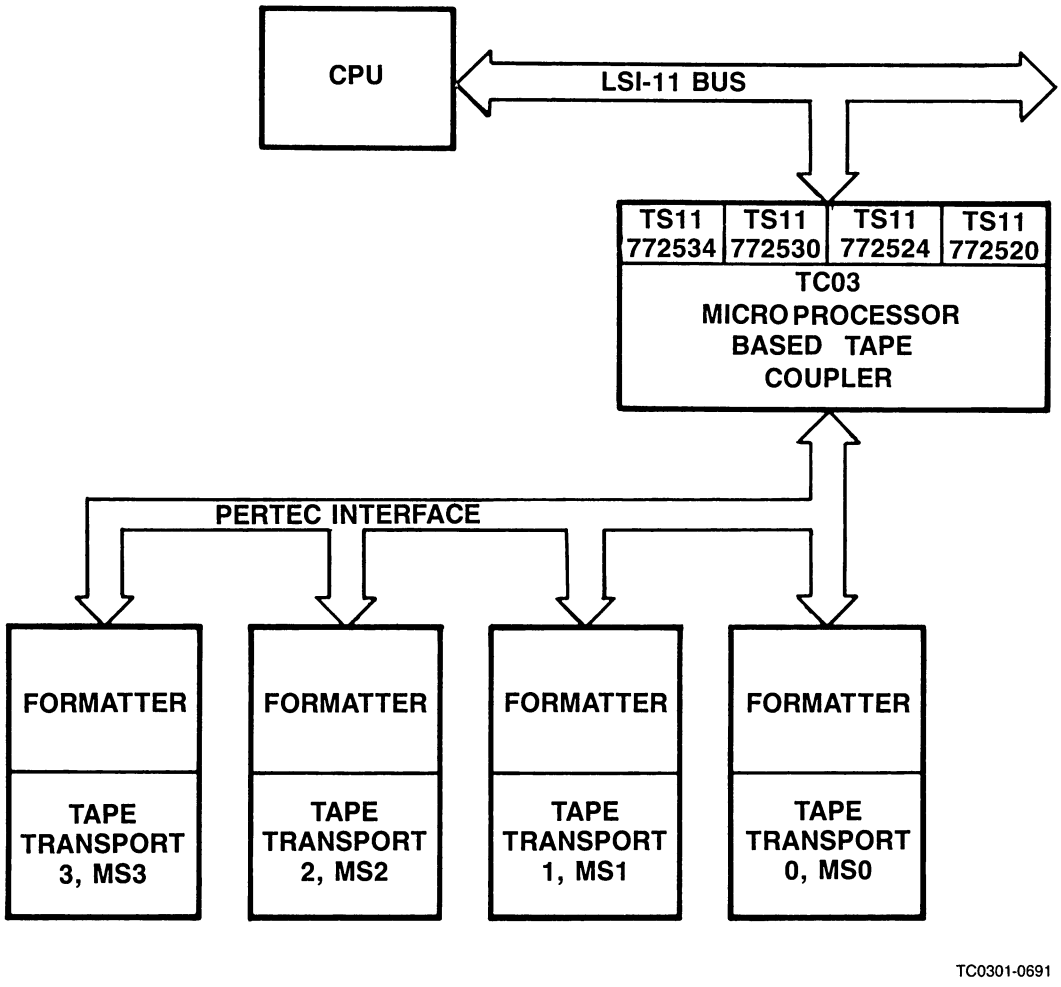


Figure 1-1. TC03 Subsystem Configuration

1.3 PHYSICAL CHARACTERISTICS

The TC03 is a microprocessor-based emulating tape coupler, located on a single quad-size, four-layer printed circuit board assembly (PCBA). The PCBA plugs directly into any LSI-11 bus slot and into connectors A, B, C, and D of the backplane, from which it draws its power. Two 50-wire flat cables connect the TC03 to the embedded formatter in the first tape transport.

1.4 SUBSYSTEM MODELS AND OPTIONS

The TC03 Tape Coupler is pictured in Figure 1-2. A single model of the TC03 is offered: the TC03. The TC03 is identified by a top-level assembly tag that is glued to one of the 2901 bit-slice

microprocessor chips on the PWB. The TC03 top level assembly number is given in Table 1-1, along with the part numbers of the items that are delivered with the TC03.

Table 1-1. Basic Subsystem Contents

Item	Qty	Description	Part Number	Comment
1	1	TC03 Tape Coupler	TC0310201-FSX	X is firmware revision
2	1	TC03 Technical Manual	TC0351001	
3	1	22-Bit Addressing Kit	CS0113001	

1.4.1 SUBSYSTEM OPTIONS

Table 1-2 lists the options that can be ordered to tailor your TC03 to your particular application.

Table 1-2. Subsystem Options

Option	Description
PD9951802-01	Backup and Restore Program (BRP). Allows image backup and restoration of disk. Compatible with the following disk/tape subsystems and all Emulex emulations of these DEC products: TS11 RK06/07 RL01/02 RM02/03/05/80 RP06 UDA50 Distributed on 0.5-inch tape, PE format with MS boot. Not available for MicroVAX.

(Continued)

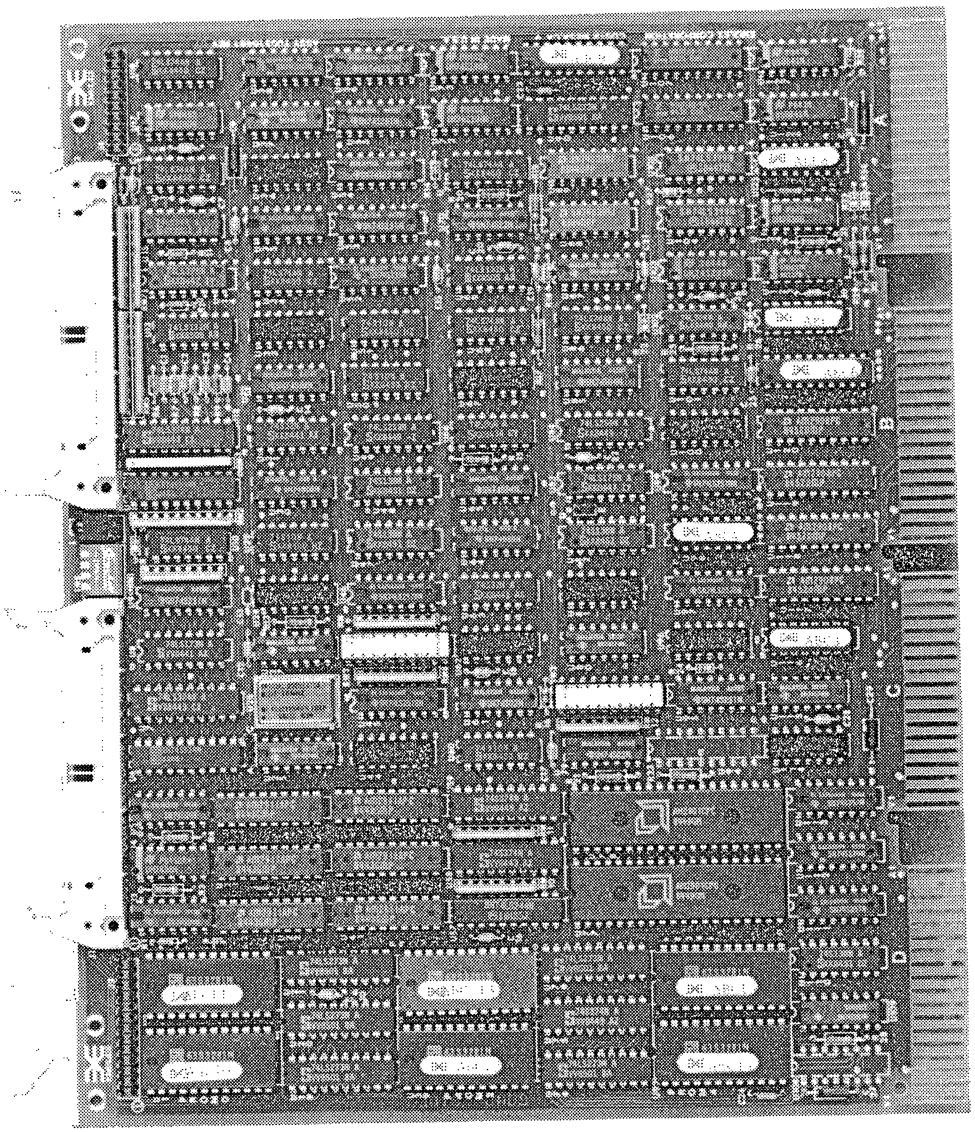
Table 1-2. Subsystem Options (Continued)

VD9960703	MicroVMS TSl1 Software Driver (TSDRIVER). This optional Emulex software driver makes your TC03 compatible with MicroVMS (MicroVAX I and II). Distributed on 5.25-inch diskette.
VX9960704	MicroVAX TSl1 Emulation Installation Diagnostic (IQTl2). An installation diagnostic for Emulex TC03 and QTl2 tape couplers; distributed on 5.25-inch diskette.

Options are specified as separate line items on a sales order. An example of a sales order is shown in Figure 1-3.

Item	Model Number	Comment/Description
1.	TC03	TC03 Tape Coupler
2.	PD9951802-01	Backup and Restore Program

Figure 1-3. Sales Order Example



TC0301-0692

Figure 1-2. TC03 Tape Coupler

1.5 FEATURES

The TC03 Tape Coupler design incorporates several features that enhance performance.

1.5.1 MICROPROCESSOR ARCHITECTURE

The TC03 Tape Coupler circuitry incorporates an eight-bit, high-speed bipolar microprocessor with AMD 2901-type bit-slice components. The microprocessor design approach provides a reduced component count, high reliability, easy maintainability, and the means to adapt a single set of hardware to a wide range of emulation capabilities through the use of microprogramming.

1.5.2 CONFIGURATION FLEXIBILITY

Configuration flexibility is provided by three DIP switch packs on the PCBA, which are used for configuring the operating characteristics of the TC03 Tape Coupler. These characteristics include device and interrupt vector address selection and other options.

1.5.3 SELF-TEST

The TC03 Tape Coupler firmware incorporates an internal self-test routine that is executed every time the computer/tape transport system is powered up. This test exercises all parts of the microprocessor, buffer, and data-handling logic. This self-test does not completely test all circuitry in the TC03, but successful completion indicates a high probability that all circuits are operational.

1.5.4 BUFFERING

The TC03 Tape Coupler includes 3.5K bytes of data buffering. It transfers to or from memory on a word basis, except for odd bytes at the start or end of the record. This feature enables the TC03 to support high-speed GCR transports.

1.5.5 DATA TRANSFER

The TC03 supports DMA (direct memory access) data transfers in 16-, 18-, or 22-bit addressing mode, or block mode transfers with an adaptive DMA algorithm. LSI-11 bus DMA speed is up to 2M bytes per second, or 3.5M bytes in block mode.

1.5.6 BOOTSTRAP OPTIONS

The TC03 supports three bootstrap options: DEC TSV05 and TK25, the Emulex bootstrap option, and the standard DEC TS11 bootstrap. The Emulex bootstrap option is a bootstrap hand-load routine that makes it possible to bootstrap easily if your system lacks a boot PROM that supports the TC03.

1.6 COMPATIBILITY

1.6.1 MEDIA COMPATIBILITY

Tapes written according to ANSI Standard X3.40-1976 are interchangeable with tapes written by tape transports with the TC03 Tape Coupler.

1.6.2 TAPE TRANSPORTS

The TC03 Tape Coupler is compatible with nine-track tape transports that can be operated in formatted mode (Pertec interface) or streaming mode (modified Pertec interface), at data densities of 800 bpi (NRZI), 1600 bpi (PE), or 6250 bpi (GCR), and at all standard tape speeds from 12.5 to 140 ips. The following transports are supported:

- Kennedy 9220 formatter with attached 9000, 9100, and 9300 drives
- Kennedy 9400 embedded formatter drives
- CDC 92181, 92185, and 92185-02
- Cipher 891 and 990

Although most of the signals in the Pertec interface are well standardized, a few of them are interpreted differently by individual tape drive vendors. The TC03 option switches are used to accommodate these differences, as explained in Section 4 of this document.

NOTE

Non-buffered CDC 92185 tape transports can be operated at 1600 bpi (PE) only.

1.6.3 DIAGNOSTICS

The TC03 Tape Coupler executes the following DEC TS11 PDP-11 diagnostics in NRZI, PE, and GCR modes:

ZTSH - Data Reliability
ZTSI - Coupler Repair Diagnostic (runs first three tests)

For a list and description of available Emulex TC03 diagnostics, see Table 1-2.

1.6.4 OPERATING SYSTEMS

The TC03 Tape Coupler is fully compatible with the TS Driver software used with the following DEC operating systems:

RSTS/E
RSX-11M
RSX-11M PLUS
RT-11
MicroVMS (see also subsection 1.4, Options)

1.7 HARDWARE COMPATIBILITY

The TC03 Tape Coupler is compatible with DEC LSI-11 and MicroVAX CPUs, and with all commands supported by the DEC TS11.

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2.1 OVERVIEW

This section contains the general specifications for the TC03 Tape Coupler, and is divided into the subsections listed in the following table:

Subsection	Title
2.1	Overview
2.2	General Specifications

2.2 GENERAL SPECIFICATIONS

Specifications for the TC03 Tape Coupler are listed and described in Table 2-1.

Table 2-1. TC03 Tape Coupler Specifications

Parameter	Characteristics
FUNCTIONAL	
Number of Tape Transport Emulations Supported	Up to 4
Tape Speeds	All standard tape speeds from 12.5 to 140 ips
Tape Transport Interface	Pertec
Media Compatibility	0.5-inch wide magnetic tape per ANSI Standard X3.40-1976; compatible with DEC TS11 format
Data Block Capacity	Up to 65,535 bytes
Priority Level	BR 4/5
Data Buffering	3.5K bytes
Data Transfer	Block-mode DMA via LSI-11 bus, 16-bit word, except for odd byte at beginning and end of record

(Continued on next page)

Table 2-1. TC03 Tape Coupler Specifications (cont'd)

Self-Test	Extensive internal self-test upon powering up
Indicator	One LED for FAULT and ACTIVITY status indications
DESIGN	High-speed bipolar microprocessor with AMD 2901-type bit-slice components
PHYSICAL	
Module	Single quad-size module
Size	Height 8.9 in. Width 10.46 in. Thickness 0.5 in.
Cables	Two 50-wire flat cables (shipping weight 3 lb)
ELECTRICAL	
Power	+5 volts (VDC), 6 amperes (A)
LSI-11 bus interface	DEC approved line drivers and line receivers
Tape Transport Interface	Open collector line drivers and TTL receivers. Maximum cumulative cable length, 30 feet (ft).
ENVIRONMENTAL	
Operating Temperature	0°C to 55°C (32°F to 131°F)
Storage Temperature	-10°C to 70°C (14°F to 158°F)
Relative Humidity	10 to 90 percent, non-condensing

Figure 2-1 shows the dimensions of the TC03 board.

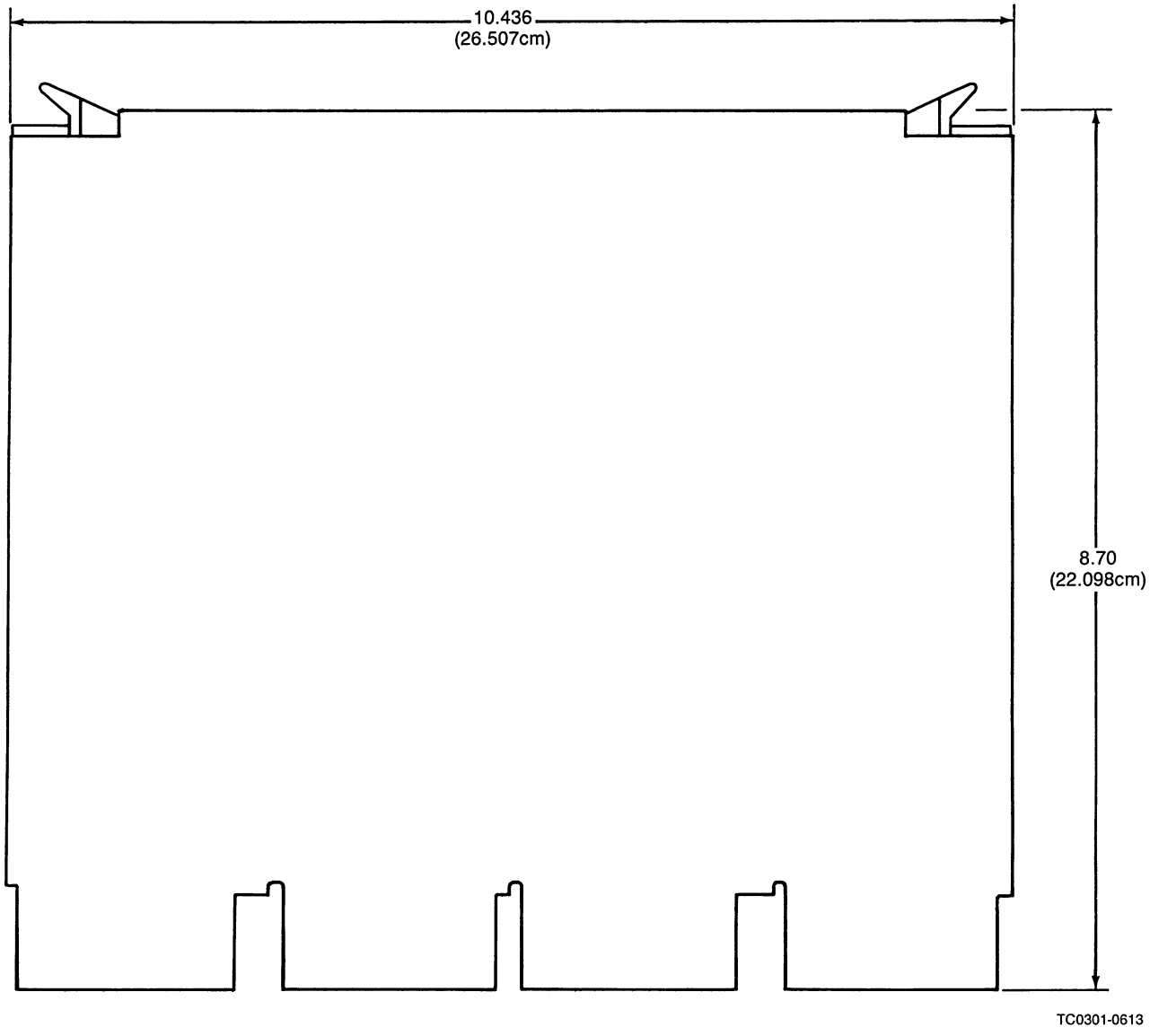

Figure 2-1. TC03 Tape Coupler Dimensions

2-3 Specifications

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Section 3
PLANNING THE INSTALLATION

3.1 OVERVIEW

This section is designed to help you plan the installation of your TC03 Tape Coupler. Taking a few minutes and planning the configuration of your subsystem before beginning its installation will result in a smoother installation with less system down time. The subsections are listed in the following table:

Subsection	Title
3.1	Overview
3.2	DEC TS11 Architecture
3.3	DEC TS11 Subsystem Configuration
3.4	TC03 Subsystem Configuration
3.5	Operating Systems, Device and Vector Addresses
3.6	Performance Considerations

3.1.1 CONFIGURATION DEFINED

As used in the computer industry, the term **configuration** is generally used to define the physical and logical arrangement of a system, or the manner in which the parts of a system relate to one another.

When used in this way, the word configuration has many implications: size (capacity, speed, bandwidth), cabling (what is hooked to what), logical arrangement (which functions are combined on which components), location (bus slot, local/remote, bus address, vector, unit address), and so on.

Many of these factors can be influenced by the user, either through the use of switches or by cabling the system appropriately. In other words, the configuration and thus the function, of a system is defined and determined by the user.

3.2 DEC TS11 ARCHITECTURE

The TC03 Tape Coupler with attached tape transport emulates the standard DEC TS11 magnetic tape subsystem. The DEC TS11 is a UNIBUS machine; the TC03 emulates it in an LSI-11 bus environment.

The TC03 can support up to four tape transports, so it actually emulates four TS11 subsystems. Because the TC03 is compatible with GCR and NRZI as well as PE mode, it provides greater flexibility than the TS11. The TC03 also includes several option switches that can be set by the user, as explained in subsection 4.4.5.

3.3 DEC TS11 SUBSYSTEM CONFIGURATION

A typical DEC TS11 subsystem is organized as shown in Figure 3-1. It consists of the following elements:

- A freestanding tape transport
- A microprocessor-controlled formatter and its power supply mounted in the transport cabinet
- A UNIBUS or LSI-11 bus interface/controller
- An I/O cable

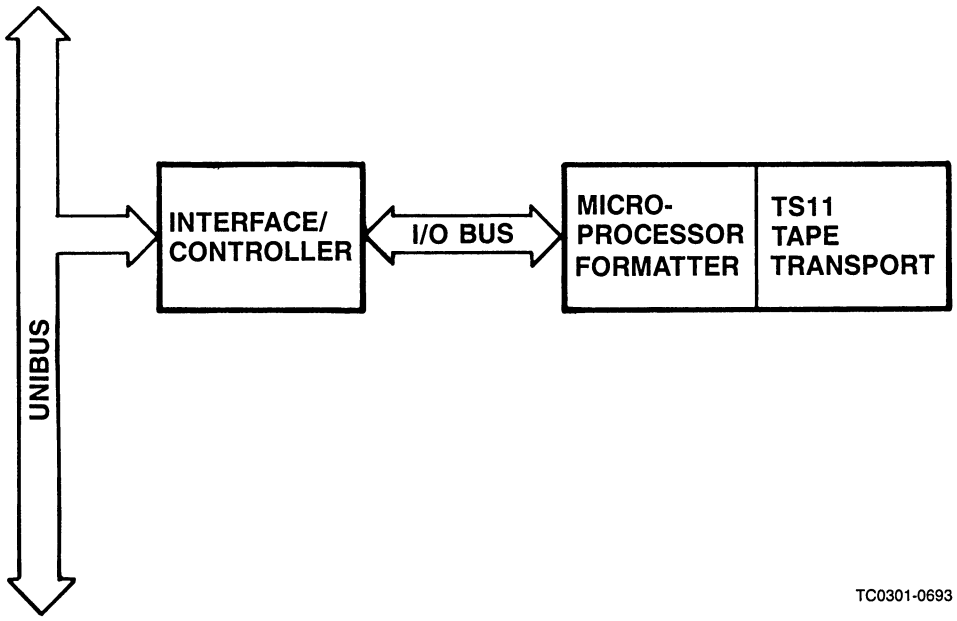

Figure 3-1. DEC TS11 Subsystem Logical and Physical Configuration

3.4 TC03 SUBSYSTEM CONFIGURATION

Figure 3-2 illustrates a typical TC03 subsystem. The TC03 emulates the TS11 in an LSI-11 bus environment. It is connected directly to the LSI-11 bus, and on the other side it uses the industry-standard Pertec interface to communicate with one to four tape transports. The TC03 performs tape control and data transfer operations for either streaming or start/stop tape transports that use NRZI, PE, and/or GCR formats. It uses PROM (programmable read-only memory) to

store instructions used by the on-board microprocessor to perform the TS11 emulation. Like the DEC system it emulates, the TC03 was designed to operate at medium speeds in moderate usage environments in a variety of applications, such as disk-to-tape backup for small to medium disks, software distribution medium, and tape interchange.

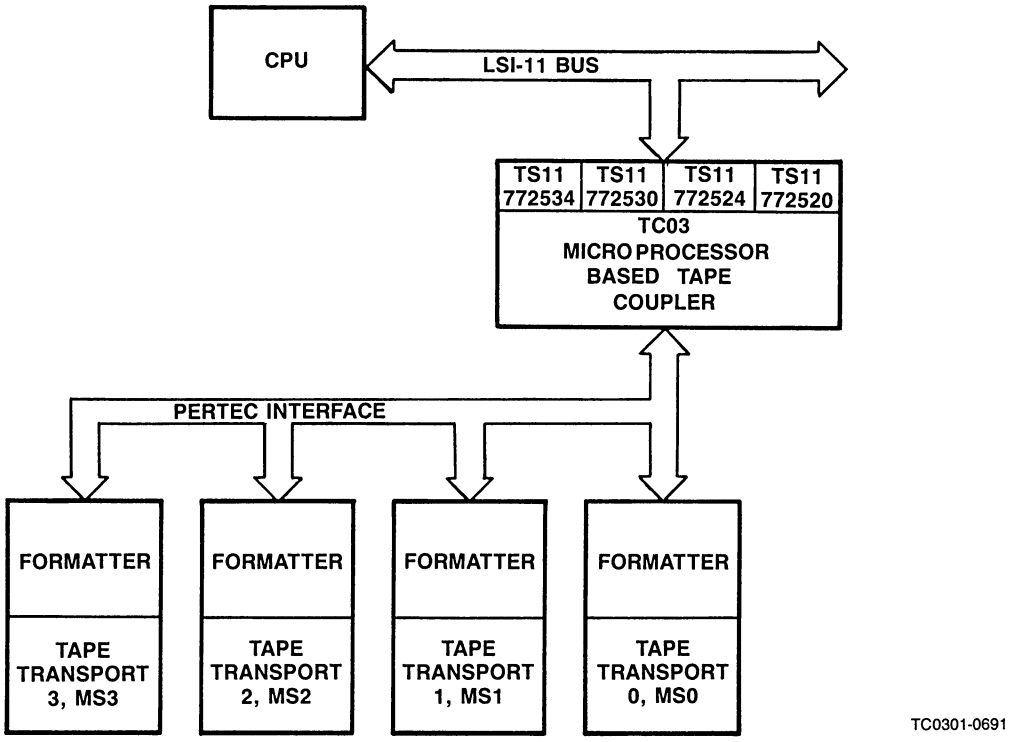

Figure 3-2. TC03 Subsystem Logical and Physical Configuration

3.4.1 Device Numbering

Up to four tape transports can be daisy-chained to each TC03, and each transport must be assigned a unique device number in the range 0 through 3. All standard DEC operating systems refer to the TS11 controller as an MS-type device. Therefore, the prefix MS is combined with the device number to form the device name: MS0, MS1, MS2, and MS3. MicroVMS adds a letter to indicate the controller: MSA0, indicates the first device on the first controller, MSB0 is the first device on the second controller, and so on.

These logical names and numbers used by DEC operating systems to reference TS11 subsystems are directly related to the base address at which the TS11 is located. The subsystem that is located at the primary base address for TS11 subsystems, 772520, is MS0. (For MicroVMS, MSA0 indicates the first device on the first controller.) The base addresses of the emulations are always contiguous (see also subsection 4.4.2):

Transport No.	Device Name	Base Address
0	MS0	772520
1	MS1	772524
2	MS2	772530
3	MS3	772534

When the TC03 and appropriate tape transports are used to emulate several TS11 subsystems, the unit addresses that are assigned to the tape transports control the relationship of a particular tape transport to a base address and, thus, to a logical name and number. For example, if the TC03 supports four tape transports with unit addresses of 0, 1, 2, and 3 respectively, it is performing four TS11 emulations. All the transports are on one formatter, which is designated as formatter 0. It need not be on transport 0, however; any address in the range 0 through 3 can be selected for the host and slave transports, irrespective of position in the daisy chain.

3.5 OPERATING SYSTEMS, DEVICE AND VECTOR ADDRESSES

A DEC host operating system can be made aware of a new device in any of three ways:

- The first technique, autoconfigure, is essentially automatic. As the operating system polls the computer's I/O device address space, it locates the TC03.
- The second technique requires that CONNECT statements be placed in a special command file that is executed each time the computer is powered up. The TC03 is manually connected using CONNECT or CONFIGURE statements.
- The third technique, interactive SYSGEN, creates a configuration file that the operating system references when the system is powered up. The user tells the operating system about the TC03 during this interactive SYSGEN procedure.

All recent versions of DEC operating systems use autoconfigure to some extent, and all try to follow the same rules. There are few differences in TS11 device treatment among DEC operating systems. Consequently, the following discussion can serve for all DEC operating systems that support the TS11. Emulex offers a TS11 driver for MicroVMS which allows the TC03 to be used in a MicroVAX environment; installation documentation is also provided. See subsection 1.4 for ordering information.

All three techniques associate a specific device-type with a **base address** and an **interrupt vector address:**

- The base address serves to distinguish the TC03 from other devices on the LSI-11 bus.

- The interrupt vector (or exception vector) is a storage location known to the system which contains the starting address of a procedure to be executed when a given interrupt or exception occurs. The system defines separate vectors for each interrupting device controller and for classes of exceptions.

DEC has reserved the base address range 772520 to 772536 for TS11-type devices on both LSI-11 and PDP-11 systems. This is enough address space to support four TS11 devices, which are adequate for most applications. If four TS11 devices are installed in that address range, the autoconfigure utilities associated with all the LSI-11 operating systems automatically detect the tape couplers and connect them to the systems. The address specified for the first TS11 must be 772520, and the addresses of additional devices must be contiguous with the preceding ones; otherwise, autoconfigure cannot find the devices.

If your application requires more than four TS11 devices, you may use three additional address ranges that the TS11 supports:

772440 - 772456
776300 - 776316
777460 - 777476

TS11 devices located in these ranges are not detected by autoconfigure, however, so they must be manually connected to operating systems by using a command file or interactive SYSGEN. See the system generation instructions for your operating system.

The standard interrupt vector address for the TC03 is 224 octal; any alternate interrupt vector address is in floating vector address space, starting at 300 octal. Instructions for programming the selected base and vector addresses into the TC03 are presented in Section 4, Installation.

3.6 PERFORMANCE CONSIDERATIONS

The Emulex TC03 Tape Coupler supports many of the low-cost streaming tape transports available today. When combined with streaming tape transports, the TC03 provides performance superior to that of the DEC TS11 subsystem at lower cost. It also provides enhancement features, such as a built-in self-test during power-up and built-in optional features that are not available on the DEC TS11 tape coupler.

Note, however, that some operating systems and CPUs are unable to transfer data to and from the TC03 rapidly enough to sustain streaming operation. Emulex recommends use of its Backup and Restore (BRP) Utility to ensure streaming mode operation for image backup and restore operations See subsection 1.4 for ordering information.

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Section 4
INSTALLATION

4.1 OVERVIEW

This section describes the step-by-step procedure for installation of the TC03 Tape Coupler in an LSI-11 bus environment. The section is divided into seven subsections, as listed in the following table:

Subsection	Title
4.1	Overview
4.2	Inspection
4.3	TC03 Tape Coupler Configuration
4.4	TC03 Tape Coupler Installation
4.5	Tape Transport Preparation
4.6	Cabling
4.7	Testing

4.1.1 SUBSYSTEM CONFIGURATIONS

This section is limited to switch setting data and physical installation instructions. No attempt is made to describe the many subsystem configurations that are possible. **IF YOU ARE NOT FAMILIAR WITH THE POSSIBLE CONFIGURATIONS, WE STRONGLY RECOMMEND THAT YOU READ SECTION 3, APPLICATION AND CONFIGURATION, BEFORE ATTEMPTING TO INSTALL THE TC03.**

When you are installing the TC03, you should make a record of the subsystem configuration and environment. Figure 4-1 is a Configuration Record Sheet, which lists the information required and shows where the data can be found. This information will be helpful to an Emulex service representative should your TC03 require service.

TC03 CONFIGURATION RECORD SHEET

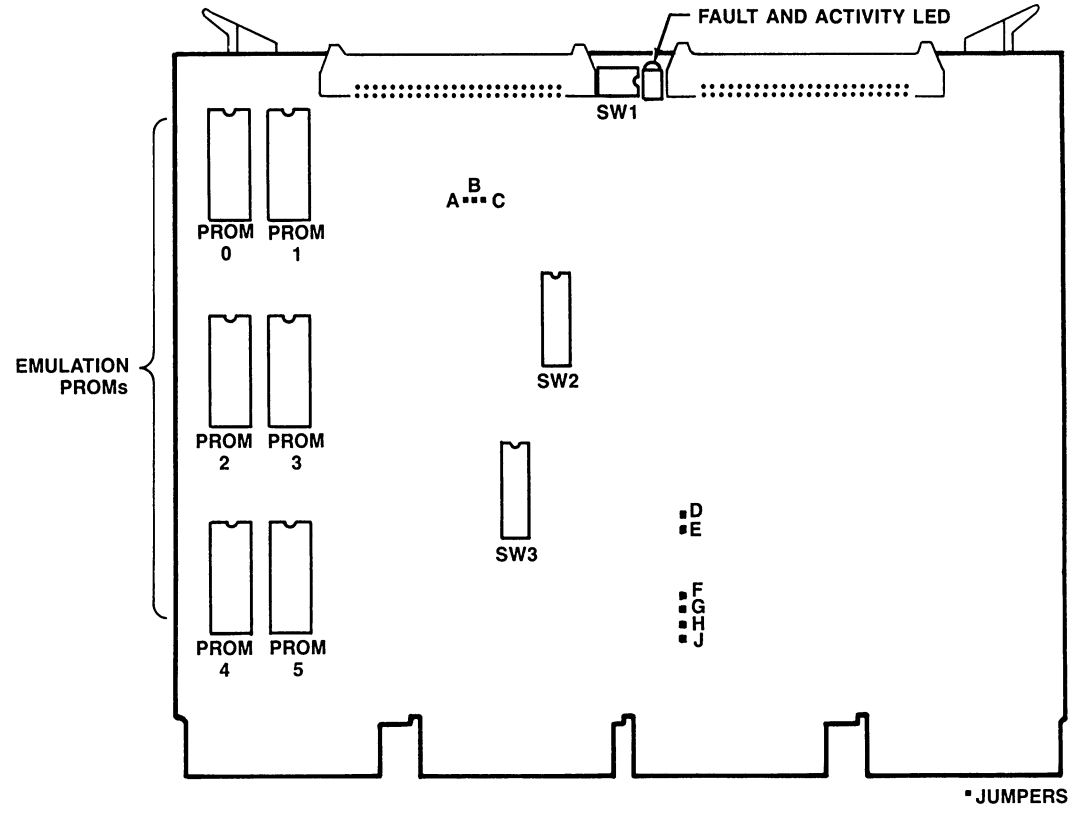
GENERAL INFORMATION

1. Host computer type _____
2. Host computer operating system _____
3. Type of memory _____
4. Amount of memory _____
5. Tape transport types _____

TC03 CONTROLLER MODULE

1. Emulation PROM numbers range from _____ to _____
2. Warranty expiration date _____
3. Top assembly number _____
4. Serial number _____
5. Jumpers connected _____
6. UNIBUS address _____
7. Interrupt vector address _____
8. Switch settings (circle 1 or 0)

	SW1				SW2										SW3									
	1	2	3	4	1	2	3	4	5	6	7	8	9	10	1	2	3	4	5	6	7	8	9	10
OFF/OPEN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ON/CLOSED	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1



Use Pencil

TC0301-0225

Figure 4-1. TC03 Configuration Reference Sheet

4.1.2 DIP SWITCH TYPES

Switch-setting tables in this manual use the numeral one (1) to indicate the ON (CLOSED) position, and the numeral zero (0) to indicate the OFF (OPEN) position.

The two DIP switch types used in this product are shown in Figure 4-2. Both are set to the code shown in the switch setting example.

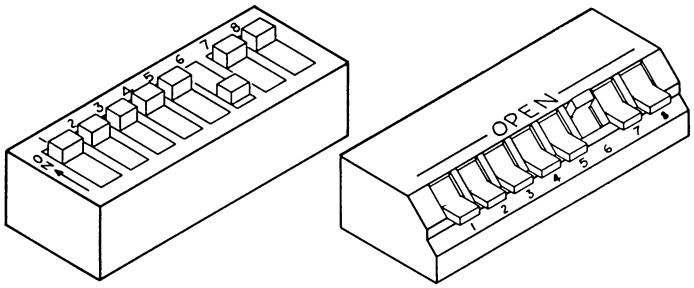


Figure 4-2. Switch Setting Example

4.1.3 MAINTAINING FCC CLASS A COMPLIANCE

Emulex has tested the TC03 Tape Coupler PCBA with DEC computers that comply with FCC Class A limits for radiated and conducted radio-frequency interference (RFI). The TC03 PCBA complies with FCC regulations and is designed to be embedded in an LSI-11 CPU system. When properly installed, the TC03 Tape Coupler system does not cause compliant computers to exceed RFI limits for Class A equipment.

To limit radiated RFI, DEC completely encloses its computer system components that could radiate or conduct RFI with a grounded metal shield. When installing system components, do nothing that could reduce the effectiveness of this shield. That is, when you have finished installing the TC03 Tape Coupler system--TC03, personality panels, blank panels (if any), bulkhead distribution panels (if any), tape transports, and shielded cables--there must be no gap in the shielding which would allow RFI radiation or conduction.

Conducted RFI is generally prevented by installing a filter in the AC line between the computer system and the AC source. Most power distribution panels of current manufacture contain suitable filters. Subsection 4.6.5 explains the procedures required to maintain shield integrity and to limit radiated RFI.

4.2 INSPECTION

Emulex products are shipped in special containers designed to provide full protection under normal transit conditions. Immediately upon receipt, the shipping container should be inspected for evidence of possible damage incurred in transit. Any obvious damage to the container, or indications of actual or probable equipment damage, should be reported to the carrier company in accordance with instructions on the form included in the container.

After unpacking the TC03 Tape Coupler, visually inspect the entire assembly for bent or broken connector pins, damaged components, or other visual evidence of physical damage. The PROMs should be carefully examined to ensure that each is firmly and completely seated in its socket. Verify that the TC03 Tape Coupler model or part number designation, revision level, and serial number agree with those on the shipping invoice. This verification is important to confirm warranty. If evidence of physical damage or identity mismatch is found, notify an Emulex representative immediately.

4.3 TC03 TAPE COUPLER CONFIGURATION

The configuration of the TC03 Tape Coupler must be established before it is installed on the LSI-11 bus in the CPU chassis. Configuration setup is made by setting switches in DIP switch packs SW1, SW2, and SW3. Component locations on the TC03 Tape Coupler PCBA are shown in Figure 4-3. Table 4-1 defines the function and factory configuration of all switches on the TC03 Tape Coupler, and Table 4-2 contains jumper definitions. The following subsections discuss configuration options.

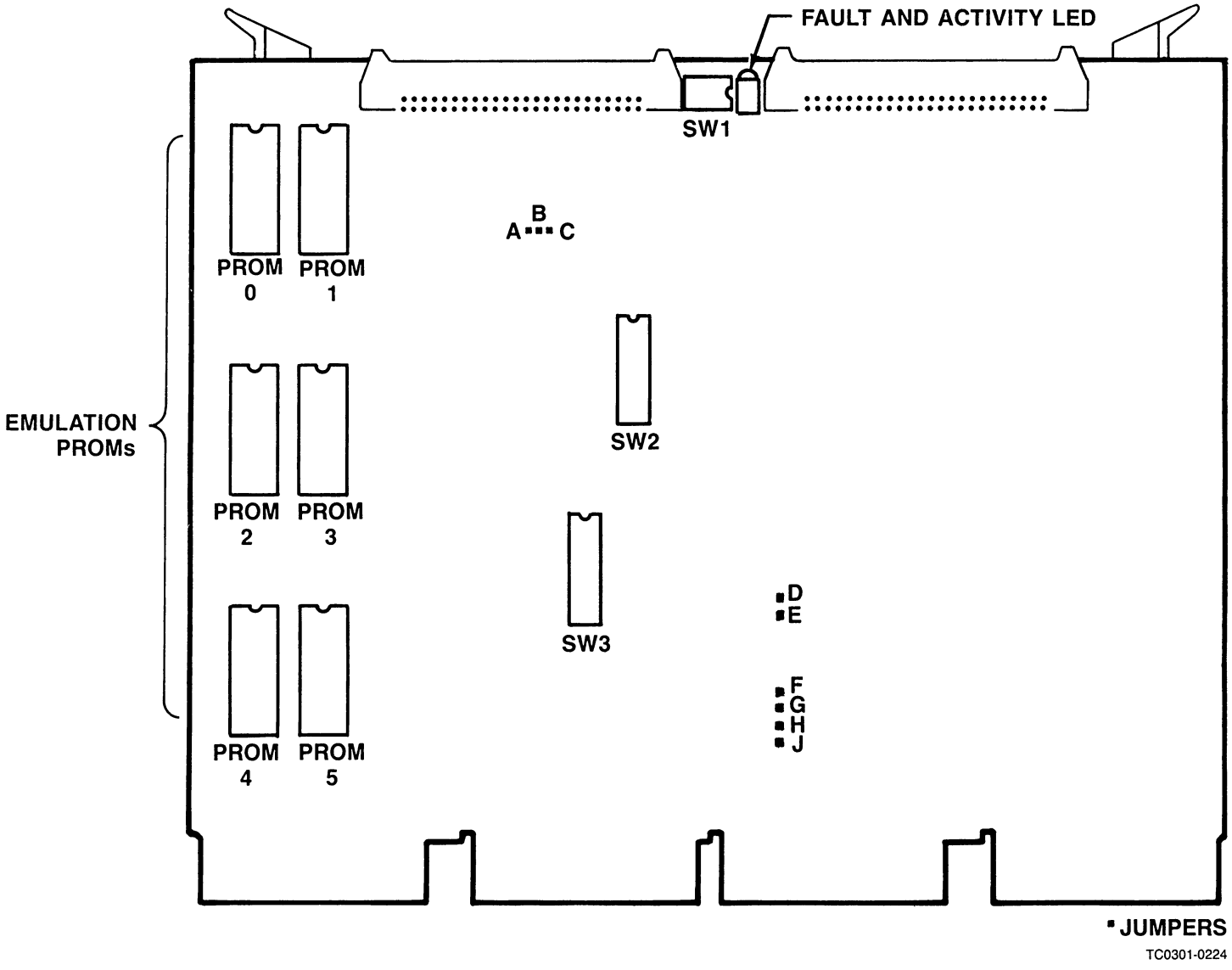


Figure 4-3. TC03 Tape Coupler Component Locations

Table 4-1. TC03 Switch Definitions and Factory Configuration

SW	OFF(0)	ON(1)	Fact	Function	Section
SW1-1	Run	Reset	OFF(0)	TC03 Tape Coupler reset	4.3.5.1
SW1-2	Disable	Enable	OFF(0)	22-bit addressing	4.3.5.2
SW1-3	Disable	Enable	OFF(0)	Remote Density Select	4.3.5.3
SW1-4	Streaming	Formatted	OFF(0)	Tape coupler mode	4.3.1
SW2-1	0	1	NS	IV (Interrupt Vector) Address Bit 2	4.3.4
SW2-2	0	1	NS	IV Address Bit 3	4.3.4
SW2-3	0	1	NS	IV Address Bit 4	4.3.4
SW2-4	0	1	NS	IV Address Bit 5	4.3.4
SW2-5	0	1	NS	IV Address Bit 6	4.3.4
SW2-6	0	1	NS	IV Address Bit 7	4.3.4
SW2-7	0	1	NS	IV Address Bit 8	4.3.4
SW2-8		224	NS	Tape transport unit 0 IV address	4.3.4
SW2-9	Disable	Enable	OFF(0)	Density Status Option	4.3.5.4
SW2-10	Disable	Enable	OFF(0)	Extended Interblock Gap	4.3.5.5
SW3-1		772520	ON(1)	Standard LSI-11 bus address	4.3.2
SW3-2			OFF(0)	Alternate LSI-11 bus address	4.3.2
SW3-3	Disable	Enable	NS	Tape transport unit 0	4.3.3
SW3-4	Disable	Enable	NS	Tape transport unit 1	4.3.3
SW3-5	Disable	Enable	NS	Tape transport unit 2	4.3.3
SW3-6	Disable	Enable	NS	Tape transport unit 3	4.3.3
SW3-7	Disable	Enable	OFF(0)	Formatted/Streaming	4.3.1.3
SW3-8	Disable	Enable	OFF(0)	No connection	
SW3-9	Disable	Enable	OFF(0)	When enabled, inhibits On-the-Fly command (for Kennedy 9000, 9100, 9300)	4.3.5.7
SW3-10	Trailing	Leading	OFF(0)	Edge of Write Strobe used to strobe data	4.3.5.8

ON(1) = closed
OFF(0) = open
NS = no standard
Fact = factory switch setting

NOTE

All unused switches must be **OFF (0)**.

Table 4-2. Jumper Definitions

Jumper Placement	Address Range Selected (Octal)
F-G F-H F-J	772440 776300 777460
Note: SW3-2 must be ON and SW3-1 OFF.	

4.3.1 TC03 TAPE COUPLER MODES

The TC03 Tape Coupler functions with streaming tape transports, formatted (start/stop) tape transports, or a combination of the two. The mode of the TC03 is determined by the positions of SW1-4 and SW3-7, as shown in Table 4-3:

Table 4-3. Tape Coupler Modes

SW3-7	SW1-4	Mode
0 0 1	0 1 x	Streaming Formatted Combination
x = Don't care		

In all three modes, you can mix transports of various densities. As the names suggest, the streaming mode supports only streaming tape transports and the formatted mode supports only formatted tape transports. In the combination mode, both streaming and formatted tape transports can be used, but be sure they are located at the appropriate transport addresses (see subsection 4.3.1.3).

4.3.1.1 Streaming Mode

When configured for operation with streaming tape drives, the TC03 can support up to four streaming drives with integral formatters. Streaming drives can operate in both start/stop and streaming modes. Start/stop operation is usually 25 ips, whereas many streaming transports stream at about 100 ips. The TC03 causes the transport to shift from start/stop mode to streaming mode when sufficient data is available to support the additional throughput rate (see also subsection 3.6). The mode shift is software transparent. When the TC03 is used with a tape drive that supports internal velocity control, the TC03 should be set in the start/stop mode.

4.3.1.2 Formatted Mode

When configured for operation with formatted (start/stop) transports, the TC03 can support up to four Pertec-compatible transports on a single formatter. The formatter address must be set to 0.

4.3.1.3 Combination Mode

When the combination mode is selected, the TC03 supports two formatted (start/stop) tape transports on a single formatter, and two streaming transports with integral formatters. Set the transport unit addresses as indicated in Table 4-4:

Table 4-4. Transport Addresses in Combination Mode

Emulation Number	Logical Name	Transport Address	Formatter Address	Transport Type
0	MS0	0	0	Streaming
1	MS1	1	1	Formatted
2	MS2	2	1	Formatted
3	MS3	3	0	Streaming

The streaming and formatted tape transports must be assigned addresses as indicated in Table 4-4. (Under MicroVMS, the logical names would be MSA0, MSB0, etc.) The formatter for the start/stop drives must have its address set to 1; FAD is asserted when the TC03 is accessing these two units.

4.3.2 TAPE COUPLER BUS ADDRESS SELECTION

The DEC TS11 tape coupler has two registers that are accessible from the UNIBUS. The operating system uses these registers to control and monitor the TS11. DEC operating systems expect to address TS11-type devices between 772520 and 772536 in the UNIBUS I/O page; four subsystems can be accommodated in that range.

The first subsystem is located at addresses 772520 and 772522 (the base address and TSSR address respectively), so this combination of addresses is known as the **primary base address** for TS11-type devices. Additional subsystems are located at alternate base addresses: 772524/6, 772530/2, and 772534/6. Note that the address pairs are contiguous.

The TC03, in combination with four tape transports, emulates four TS11 subsystems in an LSI-11 bus environment. Therefore, each address range includes starting addresses for four tape transport emulations, represented by LSI-11 bus registers.

Four address ranges are available. The first address in each range is the base address for the subsystem represented by the first tape transport unit number (0), and the starting addresses within each range are contiguous:

772520 - 772536
772440 - 772456
776300 - 776316
777460 - 777476

NOTE

If one of the alternate address ranges (772440, 776300, or 777460) is selected, the autoconfigure utility cannot locate or properly identify the TS11-type device; therefore, the Manual Connect command is used to configure the system.

These address ranges are selected by means of switch settings and/or jumper placement, as follows:

- SW3-1 ON selects the standard address range.
- SW3-2 ON, combined with the appropriate jumper placement, selects an alternate range. See Table 4-5. (SW3-1 and SW3-2 cannot both be ON at the same time.)

To enable individual emulations at specific addresses in the range 772520-772536, use switches SW3-3 through SW3-6, as explained in subsection 4.3.3.

Table 4-5 shows the interrelationship of tape transport numbers, switch settings, jumper placements, and base addresses. (The pairs of letters indicate jumper placements.)

Table 4-5. LSI-11 Bus Starting Addresses

Transport Number	SW3-1 N/A	SW3-2 F - G	SW3-2 F - H	SW3-2 F - J	Device Name	Enabling Switch
0	772520	772440	776300	777460	MS0	SW3-3
1	772524	772444	776304	777464	MS1	SW3-4
2	772530	772450	776310	777470	MS2	SW3-5
3	772534	772454	776314	777474	MS3	SW3-6

4.3.3 INDIVIDUAL TAPE TRANSPORT ENABLING

Each transport that is interfaced to the LSI-11 bus using the TC03 must be individually enabled by means of switches SW3-3 through SW3-6. Table 4-5 shows the relationship of the transport to its base address and the switch that enables it. This enabling feature is useful if a DEC TS11 is already installed in the CPU at the standard LSI-11 bus starting address.

It is desirable to place the second tape transport (the Emulex emulation) at the next available bus address. This is done by selecting the standard base address range on the TC03, assigning the new transport a unit number of 1, and turning SW3-4 ON. The other three enabling switches (SW3-3, SW3-5, and SW3-6) are left OFF to disable those base addresses.

The unit number of the tape transport must be set to correspond to the required base address. That is, if an address of 772524 is required, the transport address is set to 1 and SW3-4 is closed (ON).

4.3.4 INTERRUPT VECTOR ADDRESS

Each tape transport must have an individual interrupt vector address. In DEC operating systems, the TS11 is assigned one fixed interrupt vector (224). Interrupt vector addresses required for additional tape transports are assigned from floating interrupt vector address space. See Appendix A for instructions on determination of floating vector assignments.

When DIP switch SW2-8 is open (OFF), the interrupt vector address for unit 0 is selected by switches SW2-1 through SW2-7. The vector addresses for units 0 through 3 are contiguous, each address located four words from the one preceding it. For example, if 300 (octal) is selected as the vector address for unit 0, the vector addresses for units 1 through 3 will be 304, 310, and 314 respectively.

When DIP switch SW2-8 is closed (ON), the interrupt vector for tape transport unit 0 is forced to 224. The vectors for the other tape transports are not affected; their addresses are contiguous and their starting point is selected as described in the preceding paragraph. Figure 4-4 shows the relationship of SW2-1 through SW2-7 to the LSI-11 bus bits they control.

	Vector Address								
Octal		2			2			4	
Binary	0	1	0	0	1	0	1	X	X
Address Bit	08	07	06	05	04	03	02	01	00
Switch Setting	OFF	ON	OFF	OFF	ON	OFF	ON	X	X
Switch SW2-	7	6	5	4	3	2	1	X	X

Figure 4-4. Interrupt Vector Address Selection

Example 4-1. All four tape transports have contiguous interrupt vector addresses, starting at 224:

Unit	Base Address	Vector	Switch SW2 Setting 1 2 3 4 5 6 7 8
0	772520	224	1 0 1 0 0 1 0 0
1	772524	230	
2	772530	234	
3	772534	240	

Example 4-2. Tape transport unit 0 has an interrupt vector address of 224 (switch SW2-8 ON), but the remaining three tape transports have contiguous interrupt vector addresses, starting at 300 for tape transport unit 1:

Unit	Base Address	Vector	Switch SW2 Setting 1 2 3 4 5 6 7 8
0	772520	224	1 1 1 1 0 1 0 1
1	772524	300	
2	772530	304	
3	772534	310	

Example 4-3. Tape transport unit 0 has an interrupt vector address of 224 (SW2-8 ON), but the remaining three tape transports have contiguous interrupt vector addresses, starting at 304 for unit 1:

Unit	Base Address	Vector	Switch SW2 Setting 1 2 3 4 5 6 7 8
0	772520	224	0 0 0 0 1 1 0 1
1	772524	304	
2	772530	310	
3	772534	314	

4.3.5 OPTIONS

The TC03 tape coupler has several other option switches that allow the user to optimize it for a particular application. The options are described in the following subsections.

NOTE

Remember, some of the options apply to the Streaming mode and others to the Formatted (start/stop) mode.

4.3.5.1 Run/Reset Option

DIP switch SW1-1 allows selection of the Run/Reset option. When enabled (ON), the TC03 tape coupler is reset and initialized.

Switch	OFF	ON	Factory
SW1-1	Run	Reset	OFF

4.3.5.2 Twenty-two-bit Addressing Option

DIP switch SW1-2 allows selection of the 22-bit-addressing option. When enabled (ON), the 22-bit addressing mode is selected.

Switch	OFF	ON	Factory
SW1-2	18-bit	22-bit	OFF

To enable this option, you must also install the option IC provided with the TC03 in socket U121 on the PCBA.

To remove and replace the IC, use the following procedure:

1. Remove the installed IC from its socket by using an IC puller or equivalent tool.
2. Check the distance between the two parallel rows of pins on the IC to be installed. If the pin rows are too far apart to allow the IC to fit in the socket, perform step 3; otherwise, go to step 4.

3. Grasp the IC at its ends between your thumb and forefinger. Press one row of pins against a table top or other firm, flat surface, and gently bend the row of pins inward to allow the IC to fit the socket.

4. Orient the IC so that pin 1 is at the upper left when you are inserting the IC. (The pin 1 end of the IC is usually indicated by a cut or molded pattern in the top of the casing; the identity method depends upon the manufacturer.)

5. Carefully insert the IC in the socket. Verify that the IC is seated firmly and that no pins are bent or misaligned.

CAUTION

Some manufacturers of LSI-11 bus backplanes use the backplane lines now devoted to extended addressing for power distribution. Installing a TC03 with the 22-bit addressing option in such a system **will** damage the option IC.

4.3.5.3 Remote Density Select

DIP switch SW1-3 allows software selection of density mode. When this switch is ON, remote density select is enabled, and either high or low density mode can be selected by toggling bit 00 in the characteristic mode byte of the Set Characteristics command packet (see subsection 6.3.4.3). Note that software modification is required.

Switch	OFF	ON	Factory
SW1-3	Local select	Remote select	OFF

4.3.5.4 Density Status Option

The standard Pertec interface uses the signal INRZ to indicate 800 bpi (NRZI) mode. Some tape transports, such as the CDC 92185, Telex 5291, and STC 2920, use this line to indicate GCR mode. SW2-9 is provided to allow the use of these transports. When SW2-9 is OFF and INRZ is TRUE, the TC03 expects to find CRC and LRC characters at the end of a record. When SW2-9 is ON, the TC03 ignores the state of the INRZ signal and assumes PE or GCR mode. When SW2-9 is ON, all connected transports must be in PE or GCR mode.

Switch	OFF	ON	Factory
SW2-9	INRZ TRUE = NRZI mode	INRZ ignored	OFF

NOTE

When this option is selected, only CDC GCR streaming tape transports can be attached to the TC03.

4.3.5.5 Extended Interblock Gap Option

DIP switch SW2-10 allows selection of normal or extended Interblock Gap. The length of the interblock gap determines the maximum time within which the operating system software must issue another Read or Write command to keep the tape transport streaming. If another command is not issued within that time limit, the tape transport halts and repositions the tape.

When streaming mode is selected (SW1-4 OFF), selecting this option causes the TC03 to write longer interblock gaps. Lengthening the interblock gap increases the maximum time within which the system must issue another command, but longer interblock gaps also use more tape. Normal interblock gaps are 0.6 inch long, and the software has 2.5 milliseconds (msec) to issue another command. With extended interblock gaps, which are 1.2 inches long, the operating system has 8.5 msec in which to issue another command.

NOTE

Selecting this option may dramatically reduce storage capacity of the tape if an Extended Interblock Gap is generated for each record written.

Switch	OFF	ON	Factory
2-10	Normal gap	Extended gap	OFF

4.3.5.6 On-the-Fly Command Option

When ON, DIP switch SW3-9 inhibits On-the-Fly commands (for use with Kennedy 9000, 9100, and 9300).

Switch	OFF	ON	Factory
3-9	Enabled	Inhibited	OFF

4.3.5.7 Write Data Strobe Option

DIP switch SW3-10 allows the user to select operation on the leading or trailing edge of the Write Data Strobe pulse. It is normally open. It should be closed only to enable operation of tape transport models that need data to be output from the TC03 Tape Coupler after the **leading** edge of the Write Data Strobe pulse, instead of after the **trailing** edge of that pulse. See the tape transport manufacturer's instructions.

Switch	OFF	ON	Factory
3-10	Trailing	Leading	OFF

4.4 TC03 TAPE COUPLER INSTALLATION

4.4.1 CPU PREPARATION

Before installation of the TC03 Tape Coupler and associated tape transports, the CPU must be made accessible to the installer. To gain access to the CPU, power down the system and place the main AC circuit breaker at the rear of the cabinet in the OFF position. (The AC power indicator may remain lighted without indicating a potential hazard to the installer.)

To prepare your CPU to accept the TC03, use the following procedures:

MicroPDP/MicroVAX Preparation:

1. Power down the system by switching OFF the main AC breaker.
2. Remove the rear cover from the chassis so that the patch panel is exposed. The rear cover is held on by snap pads. Grasp the cover at the top and bottom, and pull straight back.
3. Loosen the captive screws from the patch panel using a standard screwdriver.
4. Remove the patch panel.
5. Find the flat-ribbon cable that connects the CPU module to the patch panel. For easier board installation, you may disconnect the CPU flat-ribbon cable from the patch panel.

LSI-11 Series Preparation:

1. Power down the system by switching OFF the main AC breaker.
2. Remove the cover from the chassis so that the backplane is exposed.

Do not replace the covers or patch panels until the installation is verified (subsection 4.x).

4.4.2 SLOT SELECTION

The TC03 Tape Coupler can fit into any LSI-11 bus quad slot on the LSI-11 CPU backplane. Before selecting the slot for the TC03, however, you must examine system hierarchy and architecture to ensure proper priority sequence and backplane continuity.

The TC03 can buffer up to 3.5K bytes of data; therefore, it requires less direct memory access (DMA) priority than controller devices that contain less buffering. Controllers with RK, RL, or TM11 emulations require higher DMA priority than the TC03 Tape Coupler, because they need higher priority for faster access to prevent buffer overrun. The TC03 should be installed toward the end of the NPR priority chain.

DMA continuity must be ensured by leaving no empty LSI-11 bus quad slots between PCBAs in the backplane. Several methods of preserving DMA continuity are available. For specific information regarding DMA continuity requirements, refer to the backplane or CPU user's guide.

CAUTION

Some manufacturers of LSI-11 bus backplanes use the backplane lines now devoted to extended addressing for power distribution. Installing a TC03 with the 22-bit addressing option in such a system **will** damage the option IC.

4.4.3 MOUNTING

The TC03 Tape Coupler PWB should be plugged into the LSI-11 backplane with components oriented in the same direction as the CPU and other modules. Always insert and remove the boards with the computer power OFF to avoid possible damage to the circuitry. Be sure that the board is properly positioned in the throat of the board guides before attempting to seat the board by means of the extractor handle.

4.5 TAPE TRANSPORT PREPARATION

Unpack and install the tape transport(s) as instructed in the manufacturer's manual. Position and level it in its final place before beginning installation of the TC03 Tape Coupler. This positioning allows input/output (I/O) cable routing and length requirements to be determined accurately.

Configure the tape transport(s) for the desired operating mode by using the appropriate switches on the transport operator control panel (OCP), or by issuing appropriate commands via software. Tape transport addresses (subsection 4.3.3) are sometimes selected by a thumbwheel switch on the OCP, but more frequently by switches or jumpers on one of the logic PCBAs in the tape transport.

4.5.1 DAISY CHAIN OPERATION

The TC03 supports daisy-chain operation of up to four drives. Because each drive requires its own bus address and interrupt vector location, your operating system must be set up to support as many CSR and interrupt vectors as there are attached drives. Two types of daisy-chain operation are possible:

- Multiple master formatters
- Single master formatter with multiple attached slaves

The type of daisy chain operation used depends on the tape drive vendor. The main difference is in the cabling requirements (subsection 4.6).

Because some formatted tape drives have options that are in direct conflict with one another, all drives on the daisy chain must be from the same vendor. Emulex does not support multiple-vendor daisy-chain operation. The only exception is in the case of combination formatted/streaming operations (subsection 4.6.4). In this case, the formatted and streaming drives can be from different vendors.

4.5.2 STANDARD VENDOR CONFIGURATIONS

The following table lists supported tape transports, and directs you to the appendix table that contains TC03 and tape transport switch settings.

Tape Transport	Appendix C Table
CDC 92181	C-1, C-2
CDC 92185, 92185-02	C-3, C-4
Cipher 891	C-5, C-6
Cipher 990	C-7, C-8
Kennedy 9400	C-9, C-10
Kennedy 9000F, 9100F, 9300F with 9220 formatter	C-11, C-12

4.5.3 GENERAL OPERATING RESTRICTIONS

Two restrictions apply to tape transport configurations with the TC03 tape coupler.

- Daisy-chain configurations will not support concurrent operations on multiple transports.
- For transports with data buffering or caching capabilities, Emulex recommends that a maximum transport data rate of 500K bytes per second be used, in order to prevent Data Late errors during writes to tape. The TC03 transfers a minimum of two words per DMR before giving up the bus to a competing DMA device. Many high-speed disk controllers are capable of forcing the TC03 into a continuous two-word-per-DMR state, which will cause a Data Late condition at transfer rates above 500K bytes per second.

4.6 CABLING

The TC03 communicates with the tape transports it controls through two 50-pin flat-cable connectors attached to 50-conductor flat ribbon cables. The cables are connected from connectors J1 and J2 on the TC03 to connectors on the formatter PCBA in the first tape transport in the system. All streaming tape transports have an integral embedded formatter; only the first start/stop transport in a daisy chain requires a formatter, however, because one formatter accommodates up to four transports.

After the TC03 Tape Coupler has been installed in the CPU backplane, it must be connected to the tape transports. Figure 4-5 shows tape transport cabling.

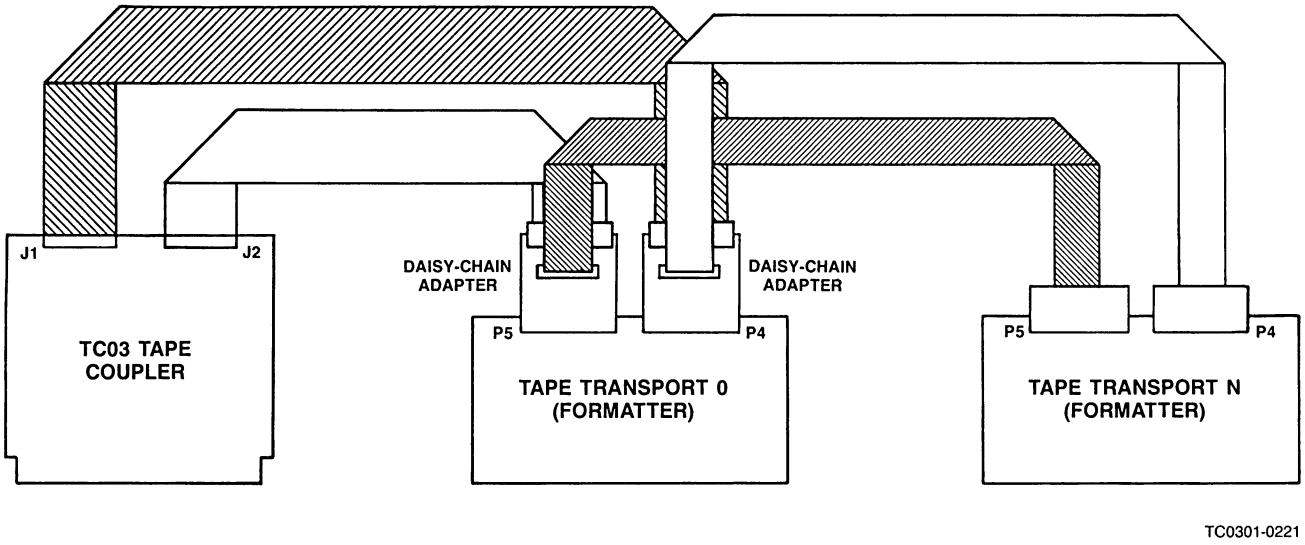


Figure 4-5. Tape Transport Interconnect Cabling

4.6.1 GROUNDING

Ground returns and shielding of all cabling within the rack/cabinet must be grounded to the cabinet, and the cabinet itself must have a sure earth ground. All cable ground returns and shielding entering the cabinet must be properly grounded, once inside the cabinet.

For proper operation of the tape transport subsystem, the tape transports **must** have a sure ground connection to the logic ground of the computer. This ground connection should be made with metal braid at least one-quarter inch wide (preferably insulated), or with AWG no. 10 wire or larger. The grounding strap or wire can be daisy-chained between the tape transports.

NOTE

Failure to observe proper grounding methods can result in marginal operation with random error conditions.

4.6.2 FORMATTED SUBSYSTEMS

The embedded formatter is an integral part of the first tape transport in the system. The TC03 Tape Coupler is connected to this formatter with the cables listed in Table 4-6.

Table 4-6. Unshielded Cables

Part Number	Description	Length (Feet)	Qty Rqd	Interface
TU1211201-01	Cable, Shielded	3	2	Pertec
TU1211201-02	Cable, Shielded	5	2	Pertec
TU1211201-03	Cable, Shielded	8	2	Pertec
TU1211201-04	Cable, Shielded	15	2	Pertec
TU1211201-05	Cable, Shielded	25	2	Pertec
TU1211201-06	Cable, Shielded	35	2	Pertec
TU1211201-07	Cable, Shielded	50	2	Pertec

The items in Table 4-6 can be ordered from your Emulex sales representative or directly from the factory:

Emulex Customer Service
3545 Harbor Boulevard
Costa Mesa, CA 92626
(714) 662-5600 TWX 910-595-2521

The cables are connected from connectors J1 and J2 on the TC03 PCBA to connectors on the formatter PCBA in the first tape transport in the system. Table 4-7 lists TC03 coupler to formatter connections. The connectors on the TC03 Tape Coupler and those on the cables are matched by aligning the arrows, which designate pin 1. The connectors on the formatter ends of the cables are aligned by matching the pin numbers molded into the face of the jack-type connector with the numbers etched on the card-edge connector over which they fit.

Table 4-7. TC03 Coupler to Formatter Connections

Manufacturer	Model	TC03 Connector J1 to:	TC03 Connector J2 to:
CDC (Tandberg)	92180	J125	J124
CDC (Keystone)	92181 (BY3A6)	P4	P5
CDC	92185	J2	J3
Cipher	F100X, F900X	P4	P5
Cipher	F880, CT-75, CT-125	P1	P2
Digi-Data	All Formatted	J4	J3
Kennedy	9000, 9100, 9300	J5	J1
Kennedy	9400	P100	P200
Kennedy	6809	J1	J2
Pertec	Formatted Start/Stop	P4	P5
Telex	9251	I/01	I/02

NOTE

Some formatters have 100-pin connectors and need an adapter that allows the two Emulex 50-pin connectors to be used. The adapter must be ordered from the formatter manufacturer.

4.6.2.1 Daisy-Chaining

Up to four tape transports can be daisy-chained from the TC03 Tape Coupler. In the case of formatted (start/stop) tape transports, usually only the first transport in the system has the embedded formatter. The rest of the transports in such a system lack a formatter, because the one embedded formatter can handle up to four transports.

The formatter for formatted tape transports is connected to the TC03 Tape Coupler as described in subsection 4.6.1. The slave tape transports are then daisy-chained from the formatter in accordance with the installation instructions supplied by the manufacturer of the tape transport. Emulex does not supply the cables that interconnect the tape transports.

NOTE

If Kennedy formatters are used in the system, the high-low switches on these formatters must also be set for the tape speeds of the individual tape transports. Set the switch banks that correspond to unused tape transports to match the speed of tape transport unit 0.

4.6.3 STREAMING SUBSYSTEMS

To install the first tape transport unit, use the instructions in subsection 4.6.1. Daisy-chaining of streaming transports is explained in the following paragraphs.

4.6.3.1 Daisy-Chaining

Unlike formatted tape transports (see subsection 4.6.1), all streaming tape transports are equipped with an integral embedded formatter. Therefore, the daisy-chaining method used for streaming tape transports differs from that used for formatted transports.

Streaming tape transports are connected by using the Emulex daisy-chain adapter (P/N TU1210402). Two adapters (one per cable) are required for each additional tape transport beyond the first to be connected to the TC03 Tape Coupler. For example, if three tape transports are to be daisy-chained, four adapters are required.

Standard Emulex cables (see Table 4-6) are used to cable between the tape transports. Termination is provided on the formatter PCBA. It may be necessary to remove or disable terminators on intermediate tape transports in the daisy chain. For complete connection details, see the manufacturer's technical manual.

4.6.4 COMBINATION SUBSYSTEMS

When the combination mode is selected, the TC03 supports two formatted (start/stop) tape transports on a single formatter, and two streaming transports with integral formatters. This daisy-chain option is further explained in subsection 4.3.1.3, and illustrated in Figure 4-6.

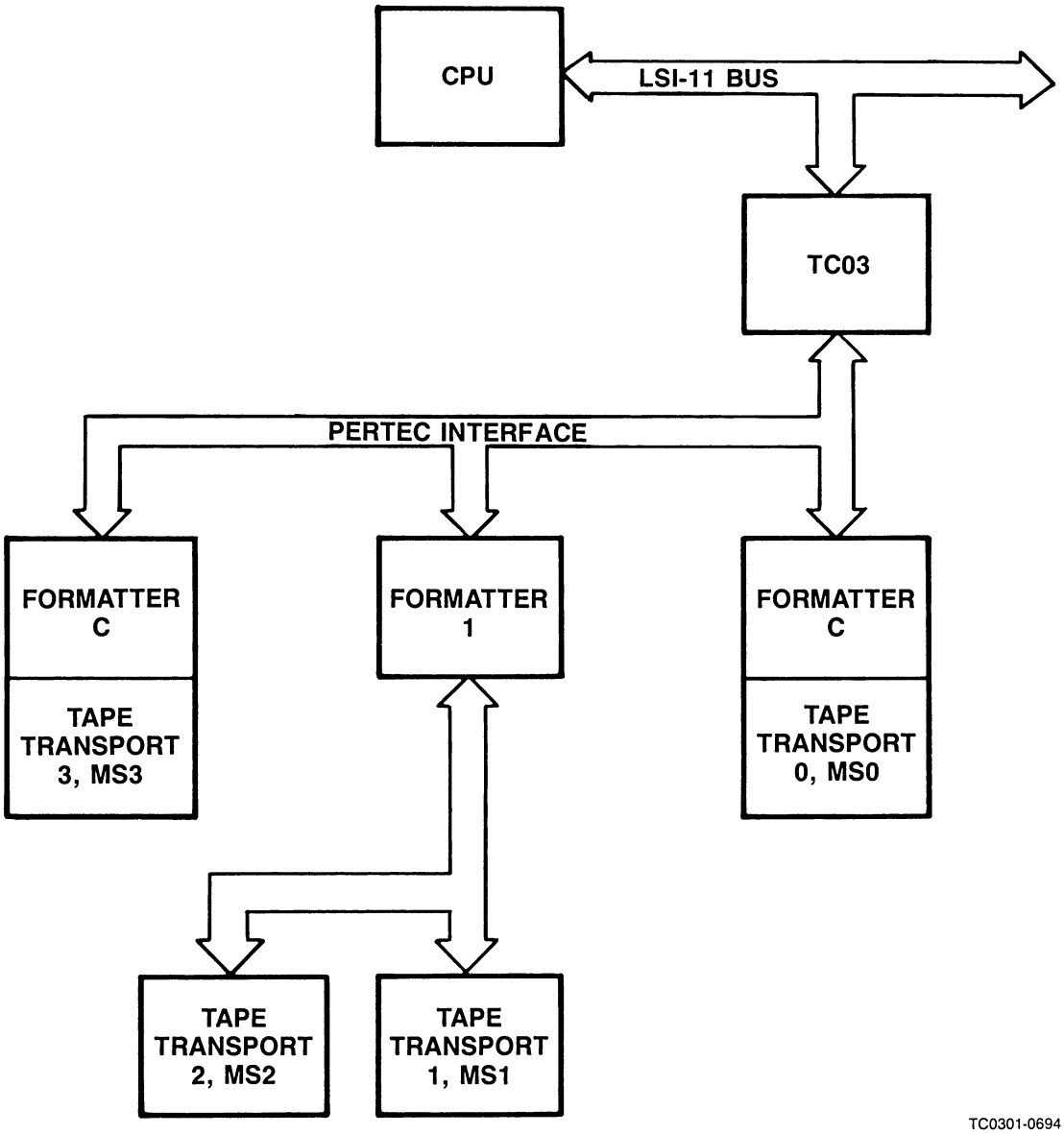


Figure 4-6. TC03 Formatted/Streaming Combination Subsystem

4.6.5 RFI SUPPRESSION

Limits for electrical RFI are governed by requirements of the Federal Communications Commission (FCC). The following subsections describe the features, use, and installation of the RFI-suppression devices manufactured by Emulex Corporation to meet FCC requirements.

4.6.5.1 RFI-Suppression Devices

RFI-suppression devices are required under the following circumstances:

- If the cabinet is of the older type that does not provide complete shielding, the cables between the Emulex product and the interconnected equipment must be shielded, even when the cables are not routed outside the cabinet.

- When peripherals controlled by the Emulex product(s) are not housed in the same equipment cabinet, the equipment must be interconnected by suitable RFI-suppression devices that ground all shielded cables entering the equipment cabinet.

The RFI-suppression devices developed by Emulex consist of suitable personality panels, unshielded cables for connections within the equipment cabinet, and shielded/jacketed cables that are routed between the cabinets. Two personality panels are required, one for each end of the shielded/jacketed cable(s). The personality panel for tape controllers and tape couplers is Emulex part number (P/N) TU210201.

For older equipment panels that lack the bulkhead with apertures for blank panels and personality panels, Emulex provides a special bulkhead distribution panel (Emulex P/N CU2220301) that can be mounted on the back of an equipment cabinet. Mounting requires four screws on each end, as shown in Figure 4-7. This distribution panel has apertures for the blank panels and personality panels.

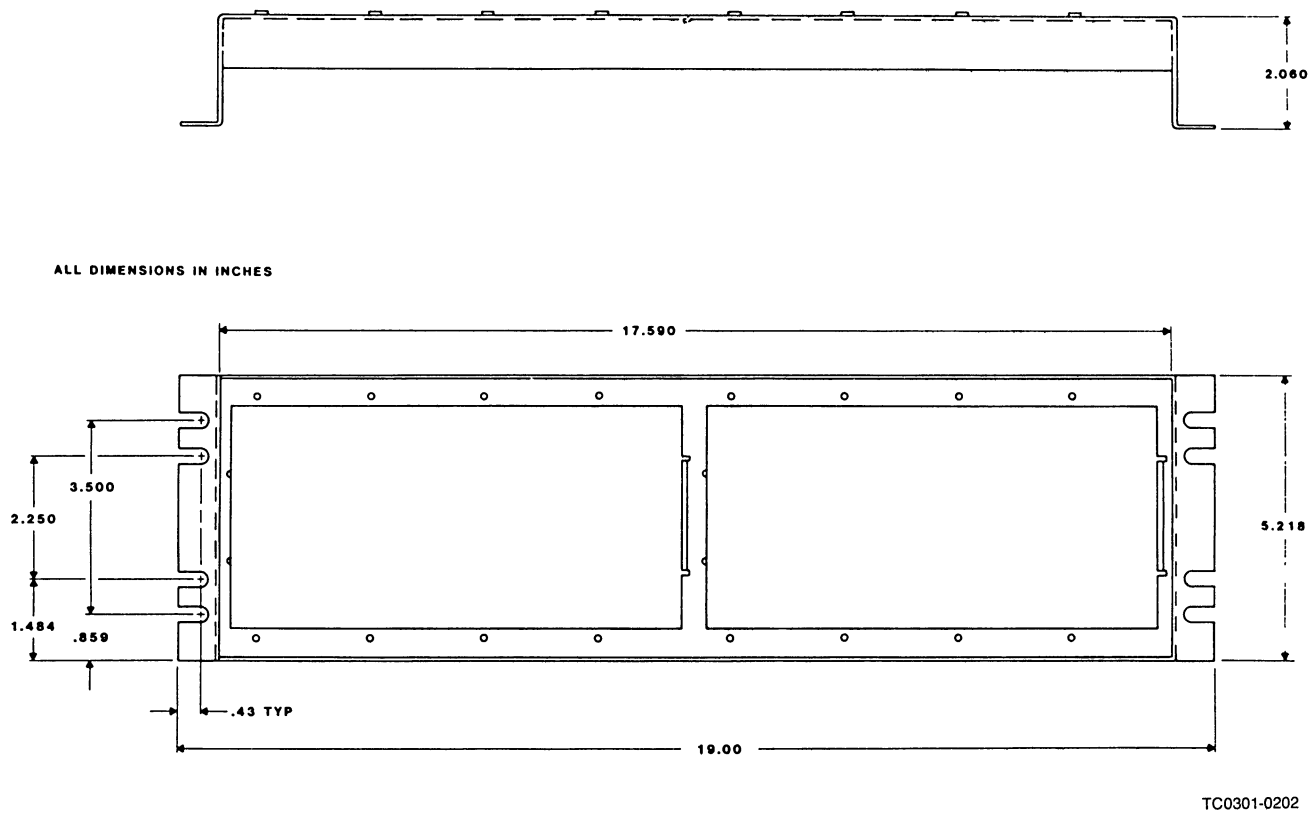


Figure 4-7. CU2220301 Bulkhead Distribution Panel

Cables and hardware details for the tape coupler installation are listed in Tables 4-6 and 4-8, with lengths expressed in feet (ft) or inches (in.) as applicable.

To install the Emulex RFI-suppression device, see Figure 4-8, and use the following procedure.

1. Open the rear bulkhead door or panel of the CPU equipment cabinet, and install the TC03 as explained in subsection 4.4.

2. Install the appropriate personality panel in a convenient aperture in the rear bulkhead of the equipment cabinet that contains the TC03. Secure it in place with eight captive screws, which should be finger-tight. Verify that there are no gaps above or below the personality panel.

3. Install two personality panels in convenient apertures in the rear bulkhead of the equipment cabinet that contains the first tape transport in the daisy chain. Secure each panel in place with eight captive screws, which should be finger-tight. Verify that there are no gaps above or below the personality panels.

4. Repeat step 3 for the remaining tape transports in the daisy chain.

5. Select a shielded interface cable (P/N TU1211202) long enough to reach from the personality panel for the TC03 to the personality panel for cable entry to the first tape transport.

6. Strip about 1 inch of shielded insulation from the end of the cable for the TC03. Cut the shield at each edge and fold it back over the insulation. Route the prepared cable ends through the appropriate slots in the personality panel, and clamp the exposed shielding securely in the personality panel (see Figure 4-8). Repeat this process for the other end of the cable.

7. Select an unshielded interface cable (P/N TU1211204) long enough to reach from connectors J1 and J2 on the TC03 to the associated personality panel in the cabinet bulkhead.

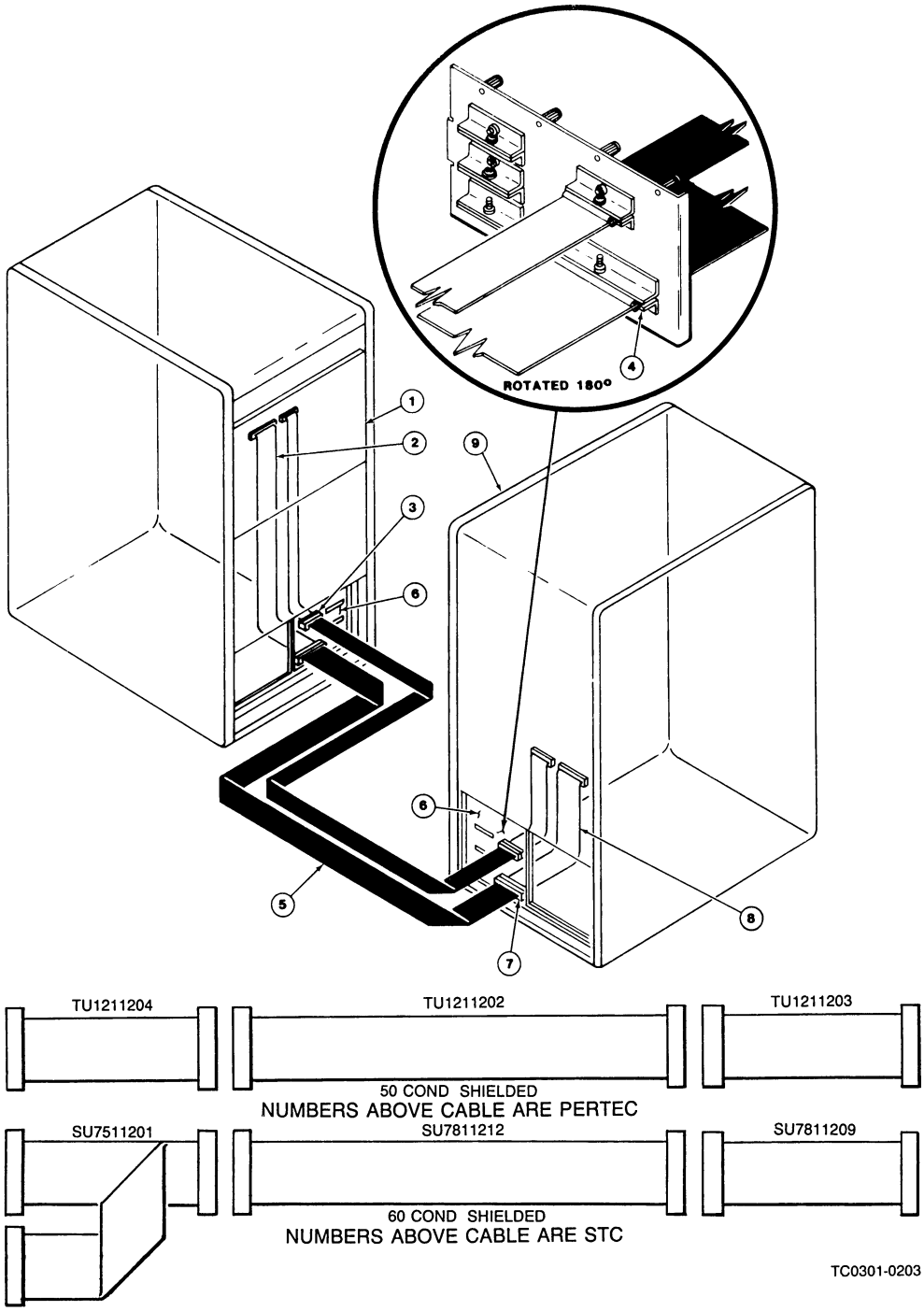
8. Align the arrows on each header of the cable connector with the arrows on each header of connectors J1 and J2 on the TC03. The arrow identifies pin 1 on each connector. Push the connectors together to make a firm connection.

9. Select an unshielded interface cable (P/N TU1211203) long enough to reach from the connector on the tape transport formatter to the associated personality panel on the rear bulkhead of the tape transport cabinet.

10. Find and align the arrows that identify pin 1 on the mating connectors at each end of the unshielded interface cable, and connect the mating connectors.

11. Interconnect the tape transports to be daisy-chained as instructed in the tape transport technical manual. Verify that the last tape transport in the daisy chain is properly terminated. If the tape transports are in separate extension cabinets, use shielded cable between cabinets, as described in the preceding steps.

12. Close the bulkhead door or panel on each equipment cabinet.



1. TC03 Tape Coupler PCBA
2. Non-shielded Extension Cable, TC03 Tape Coupler - Shielded Cable
3. Cable Connectors, TC03 Tape Coupler - Shielded Cable
4. Clamp - Shield of Shielded Cable Clamped Within
5. Shielded/Jacketed Cable, External to Equipment Cabinets
6. Personality Panels
7. Cable Connectors, Shielded Cable - Peripheral Device
8. Non-shielded Extension Cable, Shielded Cable - Peripheral Device
9. Peripheral Device

Figure 4-8. RFI-Suppression Cable Installation

Table 4-8 lists Emulex shielded cables and installation hardware for RFI suppression.

Table 4-8. Shielded Cables and Installation Hardware

Item	Part Number	Description	Length	Qty Rqd	Interface
1	TU1211202-01	Cable, Shielded	3 ft	2	Pertec
	TU1211202-02	Cable, Shielded	5 ft	2	Pertec
	TU1211202-03	Cable, Shielded	8 ft	2	Pertec
	TU1211202-04	Cable, Shielded	15 ft	2	Pertec
	TU1211202-05	Cable, Shielded	25 ft	2	Pertec
	TU1211202-06	Cable, Shielded	35 ft	2	Pertec
	TU1211202-07	Cable, Shielded	50 ft	2	Pertec
2	TU1211203-01	Cable, Extension	20 in.	2	Pertec
	TU1211203-02	Cable, Extension	40 in.	2	Pertec
	TU1211203-03	Cable, Extension	60 in.	2	Pertec
	TU1211203-04	Cable, Extension	80 in.	2	Pertec
	TU1211203-05	Cable, Extension	100 in.	2	Pertec
	TU1211203-06	Cable, Extension	120 in.	2	Pertec
3	TU1211204-01	Cable, Extension	20 in.	2	Pertec
	TU1211204-02	Cable, Extension	40 in.	2	Pertec
	TU1211204-03	Cable, Extension	60 in.	2	Pertec
	TU1211204-04	Cable, Extension	80 in.	2	Pertec
	TU1211204-05	Cable, Extension	100 in.	2	Pertec
	TU1211204-06	Cable, Extension	120 in.	2	Pertec
4	TU1210201	Personality Panel		2	All
5	CU2220301	Bulkhead Distribution Panel (Optional)		2	All

The items in Table 4-6 can be ordered from your Emulex sales representative or directly from the factory:

Emulex Customer Service
3545 Harbor Boulevard
Costa Mesa, CA 92626
(714) 662-5600 TWX 910-595-2521

4.6.5.2 Equipment Cabinet

Emulex products are installed directly in the backplane of a CPU or expansion box manufactured by DEC. There are two possible configurations in which the tape transports for the TC03 Tape Coupler system can be installed:

- In the same cabinet as the DEC CPU and TC03 Tape Coupler
- In an expansion cabinet that is separate from the cabinet in which the CPU and TC03 are installed

The equipment cabinet in which the computer equipment is installed should be a standard 19-inch-wide EIA or RETMA equipment cabinet, completely enclosed by metal. To ensure proper shielding of all equipment in the cabinet, all outer walls of the cabinet must be free of holes, except that small perforations for air exhaust are permitted.

New equipment cabinets for DEC systems have a specially fabricated rear bulkhead door or panel in which apertures have been cut. These apertures are designed for installation of blank panels, or panels with slots and associated grounding bars, which are used to provide feed-through shield grounding for cables leading to equipment mounted in other cabinets. Every aperture in the rear bulkhead panel must be filled with one of these panels, which are called "personality panels." All are the same size, as shown in Figure 4-9.

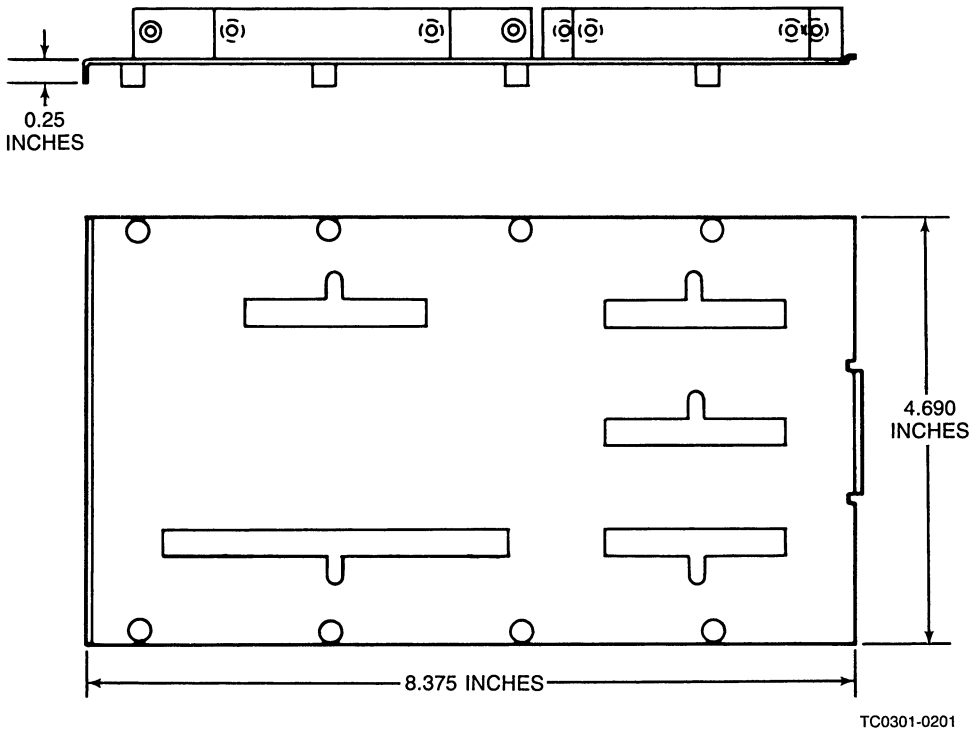


Figure 4-9. Personality Panel Dimensions

To maintain the integrity of the RFI shield, you must ensure that there is no gap above or below the replacement panel after that panel is installed. If continuity of shield integrity is maintained, no other steps are necessary to ensure RFI shield compliance for the cabinet. Conducted RFI should be prevented by the line filters that are installed by DEC in the power distribution panel for the CPU cabinet.

4.6.5.2.1 Same Cabinet. If the cabinet that houses the CPU or expansion box has enough room to include the peripheral(s) controlled by the Emulex product, those peripherals should be housed in the same cabinet. In such an installation, no shielded interconnect cables may be required, because the equipment cabinet itself provides the shielding. The main concern is installing the system so that no gaps are left in the shield.

NOTE

If the cabinet in which the TC03 and LSI-11 CPU are installed was manufactured before 1 October 1983, it may not provide sufficient shielding or filtering to prevent excessive RFI radiation or conduction. In case of complaint, it is the operator's responsibility to take whatever steps are necessary to correct the interference.

4.6.5.2.2 Separate Cabinets. If the formatter and tape transport(s) to be interfaced with the TC03 Tape Coupler PCBA are to be mounted in a cabinet separate from that of the CPU, that expansion cabinet must prevent RFI radiation by being shielded in the same way as the DEC CPU cabinet. The cable that connects to the interface in the CPU cabinet must also be shielded, because it is external to the shielded cabinet environment. An unshielded extension cable (see Table 4-8) connects the TC03 to the back of the CPU cabinet.

Emulex recommends using a hardened cabinet, such as Everest Electronic Equipment Model EH9642 with the FCC option. The Everest, like the DEC CPU cabinets, has a full-length, segmented bulkhead in the rear. One of the segments should be removed and replaced with a bulkhead distribution panel, or with a rack-mount panel that contains a blank panel and a personality panel. (These components are needed to allow the shielded cable from the TC03 Tape Coupler to be terminated.) As in the DEC cabinet, there must be no gap above or below any rack-mounted panel when the installation is complete.

To prevent the introduction of conducted RFI on the AC line that feeds the internal power supply, you must install a power distribution panel with a line filter in the expansion cabinet. A typical adequate filter is the Model 1020 EMI Filter, manufactured by Filter Concepts Corporation and included in the Model MDP110 Power Supply manufactured by Marway Products, Incorporated.

4.7 TESTING

Testing is performed both by the self-test routine in the TC03 Tape Coupler and by separate diagnostic programs.

4.7.1 SELF-TEST

When the TC03 is reset (SW1-1 ON), or if a Power-Up sequence occurs in the system in which the TC03 is installed, the TC03 automatically executes a built-in self-test of its internal logic. This self-test routine is not executed with every bus INIT condition, but only when the CPU is powered up.

The self-test takes only a fraction of a second, but during this time the FAULT/ACTIVITY LED (light-emitting diode) is lighted. This LED is located on the front edge of the TC03 PCBA. If the self-test routine is executed successfully, the LED then goes off. A steadily illuminated LED indicates that the TC03 failed the self-test routine and cannot be addressed from the CPU, because the registers in the TC03 Tape Coupler remain inaccessible. The defective TC03 Tape Coupler must then be removed and replaced or repaired before the system can be functional.

NOTE

The FAULT/ACTIVITY LED also illuminates during data transfer operations to and from the tape subsystem. This LED illumination provides a visual indication of system activity.

4.7.2 DIAGNOSTICS

To verify proper system operation, run the following LSI-11 diagnostics:

ZTSIB0	Subsystem Repair Tests 1 through 3
ZTSHC0	Reliability Diagnostic (PE mode only with CDC 92185 non-buffered)

In the following example, which demonstrates how to run the ZTSIB0 diagnostic, the prompt is shown in regular type and the user response is shown in **bold** type. The symbol **<return>** indicates the carriage return or enter key.

Boot the diagnostic media. At the dot (.) prompt, type:

.R ZTSIB0<return>

At the DR> prompt, type:

DR>**STA/TEST:1-3/FLA:PNT<return>**

Do you wish to change hardware? **Y<return>**

Enter the number of units, represented here by **n**:

UNITS **n<return>**

UNIT 0 CSR=17772522**<return>**
VEC=224**<return>**
UNIT n CSR=xxxxxx
Do you wish to change software? **N<return>**

The test runs. After two passes, type the control key and C key simultaneously:

^C

At the DR> prompt, type:

DR>**EXIT<return>**

At the dot prompt, type:

.R ZTSHC0<return>

At the DR> prompt, type:

DR>**STA/TEST:1-2/FLA:PNT<return>**

Do you wish to change hardware? **Y<return>**

Enter the number of units, represented here by **n**:

UNITS **n<return>**
UNIT 0 CSR=17772522**<return>**
VEC=224**<return>**
UNIT n CSR=xxxxxx
Do you wish to change software? **Y<return>**

The diagnostic program then asks a series of questions. Type **<return>** in response to all questions except the third question, which asks:

Do you want to print recoverable errors? **Y<return>**

The test then begins running. The test numbers are printed as each test is run. The test can be stopped at any time by typing the control and C keys simultaneously:

^C

At the DR> prompt, type:

DR>**EXIT<return>**

4.7.3 BOOTSTRAP INSTRUCTIONS

For LSI-11 and PDP-11 systems, the following hand bootstrap instructions for the TC03 should be entered by means of ODT (octal debugging tool). These bootstrap instructions do not apply to MicroVAX systems. Each entry follows an @ prompt symbol:

```
@17772522/100001<return>
@/100001<return>
@R0/0<return>
@R1/17772522<return>
@R4/2020<return>
@2000/46523<return>
@R7/0<return>
@P<return>
```

BLANK

5.1 OVERVIEW

This section describes preventive maintenance and servicing procedures for maintaining optimum performance of the TC03 Tape Coupler system. The section is divided into the following subsections:

Subsection	Title
5.1	Overview
5.2	Service
5.3	Fault Isolation
5.4	Power-up Self-diagnostic

5.2 SERVICE

Your Emulex TC03 Tape Coupler has been designed to give years of trouble-free service, and it was thoroughly tested before leaving the factory.

Should one of the fault isolation procedures indicate that the TC03 is not working properly, the product must be returned to the factory or to one of Emulex's authorized repair centers for service. Emulex products are not designed to be repaired in the field.

Before returning the TC03 Tape Coupler to Emulex, whether or not it is under warranty, you must contact the factory or the factory's representative for instructions and a Return Materials Authorization (RMA) number.

Do not return a product to Emulex without authorization. A product or component returned for service without an authorization will be returned to the owner at the owner's expense.

In the continental United States, Alaska, and Hawaii, contact:

Emulex Technical Support
3545 Harbor Boulevard
Costa Mesa, Ca 92626
(714) 662-5600 TWX 910-595-2521

Outside the United States, notify the distributor from whom the subsystem was initially purchased.

To help you efficiently, Emulex or its representative requires certain information about the product and the environment in which it is installed. During installation, you should have made a record of

the switch settings on the Configuration Reference Sheet (Figure 4-1, located in Section 4, Installation).

After you have notified Emulex and received an RMA, package the product (preferably using the original packing material) and send it **postage paid** to the address provided by the Emulex representative. You must also insure the package.

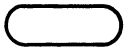
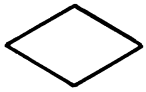
5.3 FAULT ISOLATION

The fault isolation procedure is provided in flowchart format. This procedure is based on standard troubleshooting techniques as well as the self-diagnostics incorporated into the TC03. The procedure is designed to be used if the self-test fails or if many errors are flagged by the subsystem during normal operation. (If neither of these events takes place, then it is not necessary to follow these procedures.)

Table 5-1 defines the flowchart symbols used in Figure 5-1, the fault isolation flowchart.

If the fault isolation procedure indicates that a component must be returned to Emulex, see subsection 5.2 for instructions.

Table 5-1. Flowchart Symbol Definitions

Symbol	Description
	Start point, ending point.
	Decision, go ahead according with YES or NO.
	Connector, go to same-numbered symbol on same sheet.
	Off-page connector, go to same-numbered symbol on another sheet.
	Process
	Manual operation (offline process requiring human intervention).

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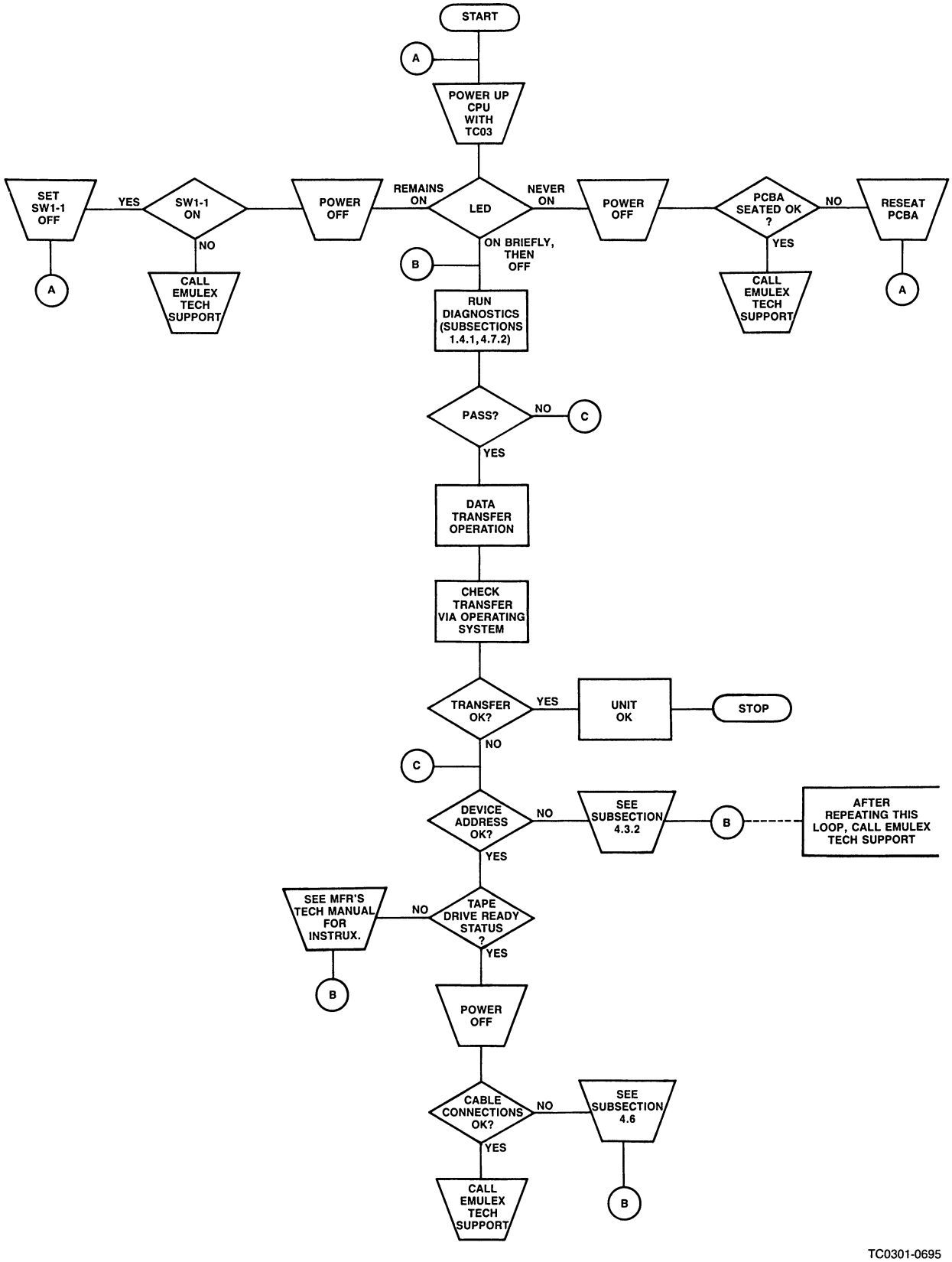

Figure 5-1. Fault Isolation Flowchart

5.4 POWER-UP SELF-DIAGNOSTIC

The TC03 executes an extensive self-diagnostic in order to ensure that the tape coupler is in good working order.

When the TC03 is reset (SW1-1 ON), or if a Power-Up sequence occurs in the system in which the TC03 is installed, the TC03 automatically executes a built-in self-test of its internal logic. This self-test routine is not executed with every bus INIT condition, but only when the CPU is powered up.

The self-test takes only a fraction of a second, but during this time the FAULT/ACTIVITY LED (light-emitting diode) is lighted. This LED is located on the front edge of the TC03 PCBA. If the self-test routine is executed successfully, the LED then goes off. A steadily illuminated LED indicates that the TC03 failed the self-test routine and cannot be addressed from the CPU, because the registers in the TC03 Tape Coupler remain inaccessible. The defective TC03 Tape Coupler must then be removed and replaced or repaired before the system can be functional.

Section 6
COUPLER REGISTERS AND PROGRAMMING

6.1 OVERVIEW

This section describes and defines the bit functions in the various registers; describes command packet formats and processing; and explains programming concepts used with a TC03 subsystem. The section is divided into four subsections, as listed in the following table:

Subsection	Title
6.1	Introduction
6.2	Coupler Registers
6.3	Command Packet Processing
6.4	Programming Operations

The TC03 emulates four DEC TS11s (see subsections 1.2 and 4.3.2); therefore, it is inaccurate to refer to a register as belonging to "the TC03," because the four register sets that the TC03 contains are not related. For example, initializing one of the subsystem emulations by writing to the appropriate TSSR does not affect the other three emulations. Nor is it necessary (nor possible) to separate TC03 commands or status from tape transport commands or status, because each register and command/message buffer set is dedicated to the individual transport. Consequently, this document uses the term **subsystem** when discussing an individual emulation.

6.2 COUPLER REGISTERS

Eight tape transport device registers are included in the TC03 subsystem, and their uses are compatible with DEC TS11 definitions. These registers are listed in the following table:

Register	Name
TSBA	LSI-11 Bus Base Address Register
TSDB	LSI-11 Bus Data Buffer
TSSR	Status Register
RBPCR	Residual Frame Count Register
XST0	Extended Status Register 0
XST1	Extended Status Register 1
XST2	Extended Status Register 2
XST3	Extended Status Register 3

For quick reference, Figure 6-1 shows the entire register set.

LSI-11BUS BASE ADDRESS REGISTER (TSBA)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
MEMORY ADDRESS															

LSI-11 BUS DATA BUFFER (TSDB)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
15	14	13	12	11	10	09	08	070	6	05	04	03	02	17	16

STATUS REGISTER (TSSR)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SC	UPE	0	RMR	NXM	NBA	A17	A16	SSR	OFL	0	0	TC2	TC1	TC0	X

RESIDUAL FRAME COUNT REGISTER (RBPCR)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RESIDUAL FRAME COUNT															

EXTENDED STATUS REGISTER 0 (XST0)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TMK	RLS	LET	RLL	WLE	NEF	ILC	ILA	MOT	ONL	IE	VCK	PED	WLK	BOT	EOT

EXTENDED STATUS REGISTER 1 (XST1)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	0	0	0	0	0	0	0	0	0	0	0	0	0	UNC	0

EXTENDED STATUS REGISTER 2 (XST2)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OPM	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EXTENDED STATUS REGISTER 3 (XST3)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	OPI	REV	0	DCK	0	0	RIB

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Figure 6-1. TC03 Tape Coupler Registers

For an explanation of LSI-11 bus registers, command packets, and command pointers, see subsection 6.4.

6.2.1 LSI-11 BUS BASE ADDRESS REGISTER (TSBA)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Memory Address															

The TSBA is a read-only 16-bit register that is read at the base address of the tape subsystem. Its contents reflect the least significant 16 bits of the 18-bit TSDB. (TSDB bits 17 and 16 are contained in TSSR bit positions 09 and 08 respectively.) The contents of TSBA are valid only after the termination of a command, which may be with or without errors. It can be read at any time, with or without the tape transport connected to the system.

When a command execution is completed, the TC03 deposits a message packet in a message buffer located in CPU memory. The contents of the TSBA can be read to determine the highest (i.e., highest-numbered) message buffer address plus 2.

6.2.2 LSI-11 BUS DATA BUFFER (TSDB)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
15	14	13	12	11	10	09	08	07	06	05	04	03	02	17	16

The TSDB is a write-only 18-bit register that is parallel-loaded from the LSI-11 bus at the base address. The TSDB can be loaded when the tape transport is bus slave by any of three types of transfers from a bus master:

- Two transfer types are for maintenance purposes (DATOB to high byte and DATOB to low byte).
- The third transfer type is for Normal (word) operation (DATO).

Whenever the TSDB is written to, the subsystem responds by asserting the SSYN signal.

6.2.2.1 Normal Operation

DATO, or word access, loads an 18-bit address into the TSDB. The address is that of a command packet located somewhere in the LSI-11 bus address space. The address is loaded into the TSDB as follows:

1. Bits <15:02> of the register are loaded with bits <15:02>, respectively, from the LSI-11 bus.

2. Bits 17 and 16 of the address are loaded with bits 01 and 00, respectively, from the LSI-11 bus.

3. Bits 01 and 00 of the address are automatically loaded with zeros by the logic in the tape transport.

Loading the TSDB causes the subsystem to fetch the command packet from the specified address. The command defined in the command packet is then executed.

6.2.2.2 Data Wraparound by Using DATOB (Odd)

Using DATOB to load the high byte (odd address) in the TSDB causes the following event sequence:

1. Bits <07:00> of the TSDB are loaded with bits <15:08>, respectively, from the LSI-11 bus.

2. Bits <15:08> of the TSDB are loaded with bits <15:08>, respectively, from the LSI-11 bus.

3. Bits 17 and 16 of the TSDB are loaded with bits 09 and 08, respectively, from the LSI-11 bus.

4. The contents of the TSDB are then loaded into the TSBA. If SSR is clear (TSSR bit 07 in zero state), an RMR error occurs (TSSR bit 12 set), but transfer is still executed and completed.

In this event sequence, the TSSR is not affected except that SSR bit 07 is cleared. To use the tape transport again, the CPU must initialize the subsystem by writing to the TSSR.

6.2.2.3 Data Wraparound by Using DATOB (Even)

Using DATOB to load the low byte (even address) in the TSDB causes the following event sequence:

1. Bits <15:00> of the TSDB are loaded with bits <15:00>, respectively, from the LSI-11 bus. (Most LSI-11 CPUs assert all zeros for bits <15:08>, except in the case of a MOVB, which extends the sign bit (bit 07) into the high byte. See the appropriate processor handbook for information regarding the MOVB instruction.)

2. Bits 17 and 16 cannot be determined.

3. The contents of the TSDB are then loaded into the TSBA.

To use the tape transport again, the CPU must initialize the subsystem by writing into the TSSR.

6.2.3 STATUS REGISTER (TSSR)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SC	UPE	SPE	RMR	NXM	NBA	A17	A16	SSR	OFL	0	0	TC2	TC1	TC0	X

The TSSR is a Read/Write 16-bit register located at base address 1777XXXX + 2. Its contents can be read at any time with or without the tape transport connected in the system. The TSSR can be updated only by the logic in the subsystem; it cannot be modified from the LSI-11 bus, except indirectly. (SPE, UPE, RMR, NXM, and SSR bit positions are cleared when the TSDB is written into by the host CPU.)

Any write to the TSSR is decoded as a Subsystem Initialize function. Initializing resets the tape transport and the TC03 Tape Coupler, regardless of the state they are in. If the tape transport is in the Online mode, initializing causes an automatic load sequence to occur which returns the tape to the BOT (beginning of tape) position.

Bit positions <14:11> and 07 are cleared only on system power-up, tape transport power-up, or subsystem initialize, or at the beginning of any Write command to the TSDB. Bit positions 15 and 07 are under control of the subsystem and can be set or cleared independently of any subsystem operation. Bit positions 10 and <06:00> are controlled by the subsystem, and the status of these bits reflects the subsystem status.

Bits <03:01> increase status reporting capability by providing the seven termination class (TC) codes listed and described in Table 6-1.

Table 6-1. Termination Class Codes

TSSR Bits <03:01>	TC Code	Message Type	Description
000	0	END	Normal Termination. This TC code indicates the operation was completed without incident.
001	1	ATTN	Attention Condition. The tape transport has changed status by going offline or coming online.
010	2	END	Tape Status Alert. A status condition occurred which can affect proper functioning of the program. Set bits that can produce TSA include TMK, EOT, RLS, and RLL.
011	3	FAIL	Function Reject. The specified function was not initiated. Set bits that can produce this rejection include OFL, VCK, BOT, WLE, ILC, and ILA.
100	4	ERR	Recoverable Error. Tape position is one record beyond what its position was when the function was begun. Suggested recovery procedure is to log the error and issue the appropriate Retry command.
101	5	ERR	Recoverable Error. Tape position has not changed. Suggested recovery procedure is to log the error and re-issue the original command.
110	6	ERR	Unrecoverable Error. Tape position has been lost. No valid recovery procedure exists, unless the tape has labels or sequence numbers.
111	7	ATTN/ERR	Not used.

On fatal errors (termination class 7), if the Need Buffer Address bit is not set (NBA = 0), the message may be valid. If the bit is set (NBA = 1), then there was no message.

The Register Modification Refused bit (RMR bit 12) status does not affect the termination class error codes, because RMR may be set on a bug-free system. The set RMR bit does, however, set Special Condition (SC) bit 15. This condition may indicate that the user tried to have the subsystem perform the next command while it was outputting an Attention Message (ATTN MSG). If RMR is set in the TSSR, the CPU must have written to the TSDB while a command was being executed.

The contents of the TSSR may not reflect the current state of the hardware if the ATTN bits are not enabled and the message buffer is not released. That is, the subsystem may be in the Offline mode while the TSSR reflects the Online mode. To keep the TSSR up to date would violate message packet protocol.

The TSSR is not cleared immediately after initialization. The microprocessor continues running to complete an automatic load sequence. When the tape is at BOT, the TSSR automatically updates.

Special Condition (SC) - Bit 15

When set, SC indicates that the last command was not completed without incident: Either an error condition was detected or an exception condition occurred. Examples of an exception condition are a file mark on Read commands, a reverse motion attempt while the tape is at BOT, or EOT (end of tape) encountered when writing.

LSI-11 Bus Parity Error (UPE) - Bit 14

When UPE is set and TC4 or TC5 is in effect, UPE indicates that the subsystem has detected a parity error in the data being transferred from the CPU memory.

Serial Bus Parity Error (SPE) - Bit 13

This bit is not used by the TC03. It is set by the TC03 at various times to conform to DEC TS11 emulation requirements.

Register Modification Refused (RMR) - Bit 12

RMR is set by the subsystem when a command pointer is loaded into the TSDB while the Subsystem Ready (SSR) bit is not set. The RMR bit may be set on a bug-free system if the ATTN interrupt bits are enabled.

Nonexistent Memory (NXM) - Bit 11

When NXM is set and TC4 and TC5 are in effect, an attempt has been made to transfer data to or from a memory location that does not exist. NXM may be set when fetching the command packet, fetching or storing data, or storing the message packet.

Need Buffer Address (NBA) - Bit 10

When the NBA bit is set, it indicates that the subsystem needs a message buffer address. NBA is cleared during the Set Characteristics command if the subsystem gets valid data. NBA is always set after subsystem initialization.

Bus Address Bits 17:16 (A17, A16) - Bits <09:08>

The status of A17 and A16 (bits 09 and 08 respectively) displays the values of bits 17 and 16 in the TSBA.

Subsystem Ready (SSR) - Bit 07

Set SSR indicates that the subsystem is not busy and is ready to accept a new command pointer.

Offline (OFL) - Bit 06

Set OFL indicates that the tape transport is offline and is not available for any tape motion commands from the TC03 Tape Coupler.

Termination Class (TC02, TC01, TC00) - Bits <03:01>

These bits provide an offset value when an error or exception condition occurs during performance of a command. Each of the eight possible values in this field represents a particular class of errors or exceptions. The termination class (TC) codes are listed and defined in Table 6-1. A TC code is used as an offset into a dispatch table for handling the error or exception condition. These bits are valid only when SC (TSSR bit 15) is set. For details about special conditions and errors, see subsection 6.4.3 and Table 6-5.

6.2.3.1 Bootstrap Command

The TC03 supports three types of bootstrap commands:

- **DEC TSV05/TK25 Command.** This bootstrap is used by all DEC LSI-11 bus boot options. It is invoked by writing a 1 to bit 15 of the TSSR, using a byte write instruction. This action arms the TC03 to rewind the tape to BOT and to space over the first record on the tape. The second record is read into memory, starting at the location pointed to by the TSBA. The actual boot takes place when the TSBA is written to. The DEC TSV05 boot program does this by clearing the TSBA, forcing the DMA to start at location 00000.

NOTE

A restriction built into this program prevents many DEC software distribution tapes from bootstrapping. After the boot block has been loaded, the program checks location 0 for the presence of a 240 (NOP) instruction. It is standard practice for DEC boot blocks to contain a NOP instruction in word 0. Therefore, the following tapes will not boot:

- RSX-11M+ stand-alone BRUSYS tapes used for operating system distribution
- ULTRIX 11 distribution tapes

If you attempt to boot a tape with the MS boot program on an LSI-11/73 (KDJ11B) CPU and get the message "NON-BOOTABLE MEDIA ON MS0," then the boot block probably does not contain a 240 in location 0. To circumvent this problem, you can load the boot program (Table 6-2) in the user area of the LSI-11/73+ boot PROM.

- **Emulex Command.** The subsystem can read the bootstrapped records from bootable tapes by using a special Emulex command. This special command does not require a command packet to be constructed.

  After power-up or bus INIT, writing the value 100001 into the TSSR twice causes the TC03 to space over the first record on the tape and read the second record into the CPU, starting at location 000000. Motion of the magnetic tape then stops. If program execution is started at location 000000, the bootstrapped record loads the CPU with the desired program from the tape.

  Table 6-2 illustrates a simple TS11 compatible bootstrap routine. Users may write their own program if they prefer.

- **Standard DEC TS11 Bootstrap.** The TC03 also supports the bootstrap routine used by standard DEC TS11 boot PROMs.

6.2.4 EXTENDED STATUS REGISTERS

The TC03 Tape Coupler includes five additional registers to provide additional status information: the Residual Frame Count Register (RBPCR) and Extended Status Registers 0 through 3 (XST0, XST1, XST2, and XST3).

The contents of these five registers are not read directly from the registers that are accessible at the LSI-11 bus interface. The

message packet, located in the system memory, contains the extended status words and is updated at the end of a command or by using a Get Status command. A message buffer must be defined to the subsystem before the extended status registers are available to the software.

Table 6-2. TS11 Bootstrap Routine

Address	Data				Code
		TSBA	=	172520	TS11 ADDRESS REGISTER ADDRESS
		TSSR	=	172522	TS11 STATUS REGISTER ADDRESS
001000	1012700 172520	START:	MOV	#TSBA,R0	GET ADDRESS OF TSBA INTO R0
001004	012701 172522		MOV	#TSSR,R1	GET ADDRESS OF TSSR INTO R1
001010	005011		CLR	(R1)	INIT AND REWIND TAPE
001012	105711		TSTB	(R1)	TEST IF 'SSR' IS SET
001014	100376		BPL	.-2	AND WAIT UNTIL IT IS
001016	012710 001064'		MOV	#PKT1,(R0)	ISSUE SET-CHARACTERISTICS COMMAND
001022	105711		TSTB	(R1)	TEST IF 'SSR' IS SET
001024	100376		BPL	.-2	AND WAIT UNTIL IT IS
001026	012710 001104'		MOV	#PKT2,(R0)	ISSUE READ OF FIRST RECORD ('MM:' BOOT)
001032	105711		TSTB	(R1)	TEST IF 'SSR' IS SET
001034	100376		BPL	.-2	AND WAIT UNTIL IT IS
001036	012710 001104'		MOV	#PKT2,(R0)	ISSUE READ OF SECOND RECORD (MS:' BOOT)
001042	105711		TSTB	(R1)	TEST IF 'SSR' IS SET
001044	100376		BPL	.-2	AND WAIT UNTIL IT IS
001046	005711		TST	(R1)	ANY ERRORS ????
001050	100421		BMI	HLT	HALT IN FRONT OF MESSAGE IF ERRORS
001052	012704 001100'		MOV	#NUM+20,R4	ADDRESS OF 'NUM'-->R4
001056	005007		CLR	PC	RESUME EXECUTION AT ZERO IF NO ERRORS
		046523(OCTAL) = MS (ASCII)			
001060	046523	NUM:	046523		
001062	000000	ZIP:	0		

Continued on next page

Table 6-2. TS11 Bootstrap Routine (Continued)

Address	Data	Code
		SET CHARACTERISTICS PACKET
001064	140004	PKT1: 140004
001066	001074'	PK
001070	000000	0
001072	000010	8.
001074	001116'	PK: MES
001076	000000	0
001100	000016	14.
001102	000000	0
		READ-DATA PACKET
001104	140001	PKT2: 140001
001106	000000	0
001110	000000	0
001112	001000	512.
001114	000000	HLT: HALT
001116		MES:

6.2.4.1 Residual Frame Count Register (RBPCR)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Residual Frame Count															

Residual Frame Count - Bits <15:00>

This register contains the octal count of residual bytes, records, file marks for Read operations, Space Records, and Skip File Marks commands. The contents are meaningless for all other commands.

6.2.4.2 Extended Status Register Zero (XST0)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TMK	RLS	LET	RLL	WLE	NEF	ILC	ILA	MOT	ONL	IE	VCK	PED	WLK	BOT	EOT

The contents of read-only register XST0 appear as the fourth word stored in the message buffer by the TC03 subsystem when a command is completed or when an attention (ATTN) condition has been detected. For termination class (TC) codes, see Table 6-1.

Tape Mark Detected (TMK) - Bit 15

When set, TMK causes termination class code 2 (TC2) and indicates that a tape mark (= file mark) has been detected during execution of a Read, Space, or Skip command. This bit is also set whenever a Write Tape Mark or Write Tape Mark Retry command is issued.

Record Length Short (RLS) - Bit 14

When set, RLS causes TC2 and indicates one of the following conditions:

- During a Read operation, the record length was shorter than the byte count.
- During a Space Record operation, a file mark or BOT was encountered before the position count was exhausted.
- During a Skip Tape Marks command execution, a BOT or double file mark (if Skip Tape Marks command was issued; see Logical End of Tape bit description) was encountered before the position count was exhausted.

Logical End of Tape (LET) - Bit 13

This bit can be set only if this mode of termination has been enabled through the use of the Set Characteristics command while the Skip Tape Marks command is simultaneously in effect. When set, LET causes TC2 and indicates one of two conditions:

- Two contiguous file marks have been detected.
- The first record encountered when moving off BOT was a file mark.

Record Length Long (RLL) - Bit 12

When set, RLL causes TC2 and indicates that the record read during a Read operation was longer than the specified byte count.

Write Lock Error (WLE) - Bit 11

When set with a TC3, WLE indicates that a Write operation was attempted while the tape transport was write locked. When set with a TC6, WLE indicates that the WRT LOCK switch was activated during execution of a Write operation.

Non-Executable Function (NEF) - Bit 10

When set, NEF causes TC3 and indicates that a command could not be executed because of one of four conditions:

- The command specified reverse tape direction, but the tape was already at BOT.
- A motion command was issued while the Volume Check (VCK) bit was set (see XST0 register bit 04 description).
- Any command, except Get Status or Drive Initialize, has been issued while the tape transport is in the Offline mode.
- A Write-type command was attempted while the tape transport was write locked (WLE bit set).

Illegal Command (ILC) - Bit 09

When set, ILC causes TC2 and indicates that the command field or the command mode field of a command that has been issued contains codes that are not supported by the TC03 subsystem.

Illegal Address (ILA) - Bit 08

When set, ILA causes TC3 and indicates one of three conditions:

- The command specifies an address with more than 18 bits.
- Register TSDB has overflowed.
- The command specifies an odd-numbered address when an even-numbered address is required.

Motion (MOT) - Bit 07

When set while the tape is moving, MOT causes TC3 and indicates that the tape was moved during the previous operation.

Online (ONL) - Bit 06

When set, ONL indicates that the tape transport is in the Online mode and operable. A change in the state of this bit causes a TC1 and an ATTN message, if the ATTN bits are enabled.

If ONL is reset to 0, it causes a TC3 if a Motion command is issued to the subsystem.

Interrupt Enable (IE) - Bit 05

The IE bit reflects the state of the Interrupt Enable condition that was supplied when the last command was issued.

Volume Check (VCK) - Bit 04

When set, VCK causes TC3 and indicates that the tape transport has changed state (Online mode to Offline mode or vice versa). VCK is always set after execution of the Initialization sequence. VCK is cleared by the set state of the Clear Volume Check (CVC) bit 14 in the command packet header word.

Phase Encoded Drive (PED) - Bit 03

When set, PED indicates that the subsystem is capable of writing and reading 1600-bpi PE data. This bit should always be set.

Write Locked (WLK) - Bit 02

When set, WLK indicates that the tape is write protected.

Beginning of Tape (BOT) - Bit 01

When set, the BOT bit indicates that the tape is positioned at the load point. An attempt to reverse tape motion or to rewind from BOT causes TC3.

End of Tape (EOT) - Bit 00

When set, the EOT bit indicates that the tape is positioned at EOT. The system Initialization sequence always resets the EOT bit (status termination during a Read operation, or TC2 during Write operation).

6.2.4.3 Extended Status Register 1 (XST1)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	0	0	0	0	0	0	0	0	0	0	0	0	0	UNC	0

The contents of read-only register XST1 appear as the fifth word stored in the message buffer by the TC03 subsystem when a command is completed or when an ATTN condition has been detected. For termination class (TC) codes, see Table 6-1.

Data Late (DLT) - Bit 15

When set, DLT causes TC4 and indicates one of two conditions:

- During a Read operation, the subsystem has attempted to enter another byte after the TC03 RAM buffer (silo) is full.
- During a Write operation, an attempt has been made to write another byte on the tape when the TC03 RAM buffer is empty.

These conditions occur whenever the latency of the LSI-11 bus on the CPU exceeds the required data transfer rate of the TC03 Tape Coupler.

Not Used - Bits <14:02> and 00

Each of these bits should always be 0.

Uncorrectable Data (UNC) - Bit 01

When set, UNC causes TC3 and TC4, and indicates that a data error has occurred during execution of a Read or Write command.

6.2.4.4 Extended Status Register 2 (XST2)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OPM	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The contents of read-only register XST2 appear as the sixth word stored in the message buffer by the TC03 subsystem when a command is completed or when an ATTN condition has been detected. For termination class (TC) codes, see Table 6-1.

Operation in Progress (OPM) - Bit 15

When set, OPM provides the tape-moving status indication.

Not Used - Bits <14:00>

Each of these bit positions should always be 0.

6.2.4.5 Extended Status Register 3 (XST3)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	OPI	REV	0	DCK	0	0	RIB

The contents of read-only register XST3 appear as the seventh word stored in the message buffer by the TC03 when a command is completed or when an ATTN condition has been detected. For termination class (TC) codes, see Table 6-1.

Not Used - Bits <15:07> and 04, 02 and 01

Each of these bit positions should always be 0.

Operation Incomplete (OPI) - Bit 06

When set with a TC6, OPI indicates one of two conditions:

- During a Read, Space, or Skip operation, about 25 feet of tape has moved past the read head without any data transitions having been detected on the tape.

- During a Write operation, about 4 feet of tape has moved past the read head without any data transitions having been detected on the tape.

Reverse (REV) - Bit 05

When set, REV indicates that the current operation has caused reverse tape motion. Reverse tape motion results from Retry commands as well as from Reverse Read, Reverse Space, and so on. The REV bit is cleared when the operation being performed is either a Rewind or an operation that involves forward tape motion.

Density Check (DCK) - Bit 03

When set, DCK indicates that the servo track identification burst (IDB) was not detected when the tape was moved forward from the BOT. Tapes with bad servo tracks cannot be written or read.

Reverse Into BOT (RIB) - Bit 00

When set with a TC2, RIB indicates that a Read, Space, Skip, or Retry command already in progress has encountered the BOT marker when moving tape in the reverse direction. The set RIB bit halts tape motion at BOT.

6.3 COMMAND PACKET PROCESSING

The command packet protocol scheme allows a TS11 emulation to provide a large amount of tape transport status and error information to the CPU while using only two words of LSI-11 address space. The command packet protocol also prevents the subsystem from updating error and status information asynchronously, that is, while the CPU is reading the error and status information.

6.3.1 BUFFER OWNERSHIP AND CONTROL

In order to allow the subsystem to use only two words of address space, the operating system software defines a set of locations in memory. These locations, called command buffers, are used to tell the subsystem which operation is to be performed. The operating system software also defines a set of locations in memory called message buffers, where the subsystem is to place the error and status information.

The CPU must give both the command buffer address and the message buffer address to the subsystem. For every command, the CPU gives

the command buffer address to the subsystem by writing the address of the command packet into the TSDB. Every time the CPU issues a Set Characteristics command, it gives the message buffer address to the subsystem.

Implementation of the ownership concept prevents the subsystem from updating the message buffer while the CPU is reading that buffer. The command buffer and message buffer can be owned by the subsystem or by the CPU, but neither buffer can be owned simultaneously by both. Ownership of the command buffer or message buffer can be transferred only by the current owner. Consequently, four types of transfer are possible:

- Command Buffer - CPU to subsystem, by CPU
- Command Buffer - Subsystem to CPU, by subsystem

- Message Buffer - CPU to subsystem, by CPU
- Message Buffer - Subsystem to CPU, by subsystem

An Initialize condition aborts any current operation and gives the CPU ownership of both the command buffer and the message buffer. During normal command processing, the ownership of both buffers passes simultaneously: first from the CPU to the TC03 subsystem (at the start of command processing, when the CPU writes a command pointer into register TSDB), and then from the subsystem to the CPU (when command execution has been completed).

Table 6-3 lists and describes event sequences that occur in transfers of buffer ownership.

Table 6-3. Event Sequences in Buffer Ownership Transfer

Buffer	Direction	Transfer Method
Command	CPU to TC03	The CPU transfers ownership of the command buffer to the TC03 subsystem by writing the address of the command buffer in register TSDB. This writing clears the SSR bit in register TSSR.
Command	TC03 to CPU	The TC03 subsystem transfers ownership of the command buffer back to the CPU by depositing a message packet (in the message buffer) that has the Acknowledge (ACK) bit set in the message header word. After the TC03 deposits the message, it sets the SSR bit in register TSSR to indicate the message is in the message buffer. If the ACK bit in the message has not been set, the CPU senses that the TC03 did not decode the contents of the command

(Continued)

Table 6-3. Event Sequences in Buffer Ownership Transfer (Cont'd)

Buffer	Direction	Transfer Method
		buffer and that the CPU still owns control of the command buffer. The command may then be re-issued by the CPU.
Message	CPU to TC03	The CPU transfers ownership of the message buffer to the TC03 subsystem by setting the ACK bit in the command buffer and then initiating the command by writing it into register TSDB. If the ACK bit in the command buffer has not been set, the TC03 senses that the CPU still owns control of the message buffer. Because the TC03 does not own control of the message buffer, when the CPU writes into register TSDB, the TC03 responds by setting the SSR bit and performing an Interrupt operation (if the IE bit is set) without sending a message.
Message	TC03 to CPU	The TC03 subsystem transfers ownership of the message buffer to the CPU by writing CPU into the message buffer and setting the SSR bit. This activity can occur at either of two times: • At the end of a command execution • When the TC03 is inactive and the Attention (ATTN) message is output. In this situation, the SSR bit is already set to logic 1 state because ATTN happens only when the TC03 is inactive. Therefore, the TC03 clears the SSR bit, outputs the message, sets SSR again, and interrupts the CPU if the IE bit was set in the Message Buffer Release command that gave control of the message buffer to the TC03. Note that, for an ATTN condition to occur, the EAI bit in the previous Set Characteristics command must have been set.

6.3.2 BUFFER CONTROL WITH ATTENTION ENABLED

An Attention (ATTN) condition is enabled when the CPU enters the appropriate characteristics mode word in the Set Characteristics command. ATTN allows the TC03 subsystem to flag exception conditions

when the TC03 is in the idle state and not executing a command. (Examples of exception conditions are a change in online/offline status of the tape transport, or microdiagnostic self-test errors in the TC03 subsystem.)

If the ATTN condition occurs and the TC03 subsystem does not own control of the message buffer, the subsystem queues the ATTN internally. When the CPU releases control of the message buffer on the next command (with the ACK bit set), the TC03 outputs the ATTN message, with the ACK bit in the message header word reset to the logic 0 state to indicate that the command was lost (except for the transfer of ownership of the message buffer to the TC03). This ATTN message indicates that the TC03 has refused to accept ownership of the command buffer, but has accepted ownership of the message buffer.

The CPU still owns control of the command buffer, because the TC03 subsystem did not accept control of that buffer. The CPU also owns control of the message buffer, which is currently filled with an ATTN message. If the CPU still needs to have the ignored command performed, it must re-issue the command (with the ACK bit set).

Exceptions to this procedure are the Set Characteristics command and the Write Subsystem Memory command, which are executed regardless of a pending ATTN condition. These exceptions are necessary to allow the software to specify a message buffer address, to control enabling of the ATTN condition, and to perform diagnostics.

Normally, the TC03 subsystem relinquishes ownership of message buffer control at the end of a command execution. If, however, the CPU is to be notified of a change in the status of the tape transport or of a microdiagnostic error while the subsystem is idle for a long time, the subsystem must own control of the message buffer for that entire period of time. To enable reception of such necessary ATTN messages, ownership of message buffer control is transferred to the subsystem via the Message Buffer Release command. This special command tells the subsystem not to give ownership of message buffer control to the CPU at the end of the command execution.

The TC03 subsystem does not output a message at the end of the Message Buffer Release command. It updates the contents of register TSSR (with the SSR bit set), and then interrupts the CPU if the IE bit was set in the command and if such an interrupt was enabled by the set EAI bit in the previous Set Characteristic command. The subsystem then retains ownership of message buffer control until an ATTN condition is detected. In this condition, the CPU owns control of the command buffer and the subsystem owns control of the message buffer.

When an ATTN condition is detected, the TC03 subsystem performs the following event sequence:

1. It clears the SSR bit.

2. It outputs the ATTN message, but with the ACK bit cleared (not set), because the subsystem is not responding to a command.

3. It sets the SSR bit.

4. It interrupts the CPU if the IE bit in the Message Buffer Release command has been set.

5. When the subsystem outputs the ATTN message, ownership of message buffer control passes to the CPU, which then owns control of both the command buffer and the message buffer.

The TC03 subsystem cannot send another ATTN message to the CPU until the CPU issues a command packet that contains a set ACK bit (see subsection 6.3.3), which releases ownership of the message buffer that contains the ATTN message.

If the CPU has issued a Message Buffer Release command and needs to execute another command, but has not received an ATTN message from the subsystem (which still owns control of the message buffer from the Message Buffer Release command), the CPU can issue a command without the ACK bit set in the command buffer. At the time the new command is issued, the CPU does not own control of the message buffer, so it cannot release the message buffer. If the CPU does set the ACK bit, nothing happens, except that the CPU might miss an ATTN message from the subsystem if the subsystem is sending an ATTN message at the same time that the CPU is issuing the new command.

It is possible (but not likely) that the CPU might attempt to issue a new command at or near the same time that the subsystem attempts to output an ATTN message. Therefore, the CPU should not set the ACK bit, because it does not own control of the message buffer. If the CPU writes into register TSDB while the SSR bit is clear, during an attempt by the subsystem to deliver an ATTN message, the RMR error status bit is set and that command is ignored by the subsystem. The ATTN message must not have the ACK bit set, because the subsystem does not own control of the command buffer.

NOTE

The RMR bit can be set in this way on a bug-free system. All other means of setting the RMR bit indicate a software bug in which the CPU has attempted to execute a command before the previous command execution was finished.

If the command from the CPU was lost because the subsystem was outputting an ATTN message, the IE and VCK bits (XST0 <05:04>

respectively) are not updated. If the command from the CPU was rejected (Illegal Command, etc.) and not ignored, the IE and VCK bits are updated to the start of the rejected command.

Message packet protocol may be violated if the subsystem detects an error (NXM, memory parity error, serial bus parity error, or I/O silo parity error) during the reading in of the message packet. When one of these errors occurs, the subsystem always sends a failure message (because the message packet is not reliable).

The system software should be written so that no crash occurs if the TC03 subsystem interrupts while the CPU is servicing an interrupt message from another TC03 subsystem. A system crash may occur, but only if the subsystem receives a fatal hardware error.

6.3.3 COMMAND PACKET/HEADER WORD

15	14	12	11	08	07	05	04	00
CTL	Device Dependent		Command Mode		Packet Format 1		Command Code	

	C	O	S													
ACK	V	P	W	0	0	M	M	IE	O	O	0	C	C	C	C	
	C	P	B													

The command packet header word is shown above and the bit functions are described in the following paragraphs. Bits in the fields for the command mode and command code are listed and defined in Table 6-4.

Table 6-4. Command Code and Command Mode Field Definitions

Command Code Field	Command Name	Command Mode Field	Mode Name
00001	Read	0000	Read next (forward)
		0001	Read previous (reverse)
		0010	Reread previous (Space Reverse, Read Forward)
		0011	Reread next (Space Forward, Read Reverse)
00100	Set Characteristics	0000	Load message buffer address and set device characteristic
00101	Write	0000	Write data (text)
		0010	Write data retry (Space Reverse, Erase, Write data)
00110	Write Subsystem Memory	0000	Not supported
01000	Position	0000	Space Records forward
		0001	Space Records reverse
		0010	Skip Tape Marks forward
		0011	Skip Tape Marks reverse
		0100	Rewind
01001	Format	0000	Write Tape Mark
		0001	Erase
		0010	Write Tape Mark entry (Space Reverse, Erase, Write Tape Mark)
01011	Initialize	0000	Tape transport initialize
01111	Get Status Immediate	0000	Get status (END message only)

Acknowledge (ACK) - Bit 15

This bit is set when a command is issued and the CPU owns the message buffer. Set ACK informs the subsystem that the message buffer is available for any pending or subsequent message packet(s). Set ACK passes ownership of the message buffer to the subsystem.

Device Dependent Field - Bits <14:12>

The set state of these bits causes the functions defined in the following table:

Bit	Name	Function
14	CVC	Clear Volume Check
13	OPP	Opposite (reverse execution sequence of Reread commands)
12	SWB	Swap Bytes

Command Mode Field - Bits <11:08>

The bits in this field extend the command code and allow extended device commands (Seek, Rewind, Erase, Write Tape Mark, etc.) to be specified. Definitions for the bits in this field are listed in Table 6-4.

Packet Format #1 Field - Bits <07:05>

The bits in this field define the two values listed in the following table:

Bit 07	Values 06	05	Definition
0	0	0	One word header: interrupt disable
1	0	0	One word header: interrupt enable

Command Code Field - Bits <04:00>

Bits <04:03> of this field determine the format and length of the command packet. The states of these bits are listed and defined in the following table:

Code Bits 04	03	02	01	00	Definition
0	0	X	X	X	Four words (header, two word address, count)
0	1	X	X	X	Two words (header, parameter word), or one word (header)

Bits in the command code and command mode fields are listed and described in Table 6-4.

The Swap Byte (SWB) bit in the command packet header word (bit 12) instructs the subsystem to alter the sequence of storing and retrieving bytes from CPU memory. When SWB is asserted (set to logic

1), an industry-compatible sequence (beginning with an even byte) is used. When SWB is cleared (reset to logic 0), the byte swap sequence begins with an odd byte.

NOTE

This SWB function only serves Data Transfer operations. The state of SWB is ignored for all other functions.

Figures 6-2 and 6-3 show the memory positions for the bytes as they are read from or written on the tape in a Byte Swap sequence. In these figures, the bytes of data in the record block on tape are numbered from 0. Byte 0 is always the data byte at the beginning of the data block, that is, the part of the data block closest to BOT.

NOTE

When read in reverse, the first data byte read is the last data byte of the sequence written. The Read Reverse command stores this first data byte in the last buffer position; the next data byte is stored in the next-to-last buffer position, and so on. The result is that data are placed in memory in the right order when the contents of the buffer are read sequentially.

SWAP BYTES = 0
BUFFER ADDRESS = 1000
BYTE COUNT = 10(8)
BLOCK SIZE = 10(8) BYTES

1000	1	0
1002	3	2
1004	5	4
1006	7	6

SWAP BYTES = 1
BUFFER ADDRESS = 1000
BYTE COUNT = 10(8)
BLOCK SIZE = 10(8) BYTES

1000	0	1
1002	2	3
1004	4	5
1006	6	7

SWAP BYTES = 0
BUFFER ADDRESS = 1001
BYTE COUNT = 10(8)
BLOCK SIZE = 10(8) BYTES

1000	0	
1002	2	1
1004	4	3
1006	6	5
1010		7

SWAP BYTES = 1
BUFFER ADDRESS = 1001
BYTE COUNT = 10(8)
BLOCK SIZE = 10(8) BYTES

1000		0
1002	1	2
1004	3	4
1006	5	6
1010	7	

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Figure 6-2. Byte Swap Sequence, Forward

SWAP BYTES = 0
BUFFER ADDRESS = 1000
BYTE COUNT = 10(8)
BLOCK SIZE = 10(8) BYTES

1000	1	0
1002	3	2
1004	5	4
1006	7	6

SWAP BYTES = 1
BUFFER ADDRESS = 1000
BYTE COUNT = 10(8)
BLOCK SIZE = 10(8) BYTES

1000	0	1
1002	2	3
1004	4	5
1006	6	7

SWAP BYTES = 0
BUFFER ADDRESS = 1001
BYTE COUNT = 10(8)
BLOCK SIZE = 10(8) BYTES

1000	0	
1002	2	1
1004	4	3
1006	6	5
1010		7

SWAP BYTES = 1
BUFFER ADDRESS = 1001
BYTE COUNT = 10(8)
BLOCK SIZE = 10(8) BYTES

1000		0
1002	1	2
1004	3	4
1006	5	6
1010	7	

SWAP BYTES = 0
BUFFER ADDRESS = 1000
BYTE COUNT = 7
BLOCK SIZE = 7 BYTES

1000	1	0
1002	3	2
1004	5	4
1006		6

SWAP BYTES = 1
BUFFER ADDRESS = 1000
BYTE COUNT = 7
BLOCK SIZE = 7 BYTES

1000	0	1
1002	2	3
1004	4	5
1006	6	.

SWAP BYTES = 0
BUFFER ADDRESS = 1001
BYTE COUNT = 7
BLOCK SIZE = 7 BYTES

1000	0	
1002	2	1
1004	4	3
1006	6	5

SWAP BYTES = 1
BUFFER ADDRESS = 1001
BYTE COUNT = 7
BLOCK SIZE = 7 BYTES

1000		0
1002	1	2
1004	3	4
1006	5	6

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Figure 6-3. Byte Swap Sequence, Reverse

6.3.4 COMMAND PACKET EXAMPLES

This subsection contains examples of command packets and information about operating programs that are used in the TC03 subsystem.

Each command packet contains four words. All four words are read in, even if the command requires only one word (Rewind) or two words (Space). The command packet must have correct parity, because the subsystem rejects a command packet on the basis of errors in the unused words. The command packet examples are presented in the order listed in the following table:

Command Packet	Figure	Subsection
Get Status	6-4	6.3.4.1
Read	6-5	6.3.4.2
Set Characteristics	6-6	6.3.4.3
Write	6-7	6.3.4.4
Position	6-8	6.3.4.5
Format	6-9	6.3.4.6
Control	6-10	6.3.4.7
Initialize	6-11	6.3.4.8

6.3.4.1 Get Status Command

This command causes a message packet to be deposited in the message buffer area to update the extended status registers. Because the TC03 subsystem hardware automatically updates the extended status registers after execution of any command (except the Message Buffer Release command), the Get Status command should be issued only for one of the following conditions:

- The TC03 subsystem has been left idle for some time.
- An extended status register update is desired without performing a Tape-Motion command.

Words, fields, and bits in the Get Status command packet are shown in Figure 6-4.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEVICE DEP.			MODE CODE				FORMAT #1			COMMAND CODE				
ACK	CVC	0	0	0	0	0	0	IE	0	0	0	1	1	1	1
NOT USED															

MODE CODE: 0000 = GET STATUS (END MESSAGE ONLY)

Figure 6-4. Get Status Command Packet

6.3.4.2 Read Command

The Read command has four normal modes: Read Forward, Read Reverse, Reread Previous, and Reread Next. In all modes, the Read operation is assumed to be performed on a record of known length. Therefore, the correct record byte count must be known.

If the byte count is correct, normal termination occurs. If the record is shorter than the byte count, the Record Length Short (RLS) bit is set and a Tape Status Alert (TSA) termination occurs (see TC2 in Table 6-1). If the record is longer than the byte count, the Record Length Long (RLL) bit is set and a TSA termination occurs.

Any Read operation that encounters a file mark does not transfer any data. When a file mark is encountered during a Read operation, the Tape Mark (TMK) and RLS bits are set, and a TSA termination occurs.

Read Reverse operations that run into the BOT marker cause the Reverse Into BOT (RIB) bit to be set and a TSA termination to occur. In this situation, tape motion stops at BOT. If a Read Reverse command is issued while the tape is already at BOT, the Non-Executable Function (NEF) bit is set and no tape motion occurs.

Words, fields, and bits in the Read command packet are shown in Figure 6-5.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEVICE DEP.			MODE CODE				FORMAT #1			COMMAND CODE				
ACK	CVC	OPP	SWB	X	X	X	X	IE	0	0	0	0	0	0	1
A15	LOW ORDER BUFFER ADDRESS														A00
0	HIGH ORDER BUFFER ADDRESS									A21	A20	A19	A18	A17	A16
BUFFER EXTENT (BYTE COUNT) (16-BIT POSITIVE INTEGER)															

Figure 6-5. Read Command Packet

NOTE

Bits <A21:A18> are used only when 22-bit addressing is enabled (see subsection 4.5.5.2).

If the OPP bit (header word bit 13) is set, the event sequence that occurs in execution of a Reread-type command is altered:

- Reread Previous, which is normally a Space Reverse operation followed by a Read Forward operation, becomes a Read Reverse followed by a Space Forward.
- Reread Next, which is normally a Space Forward operation followed by a Read Reverse operation, becomes a Read Forward followed by a Space Reverse.

Reading data in the reverse direction with a correct byte count places the data in memory correctly (as if the record were read in the forward direction), not in reverse order. This feature allows data to be placed correctly in memory on one retry (Read Reverse). During this operation, data are placed in the data buffer in the reverse order (highest-numbered address first); the starting address is calculated by adding the byte count to the address specified in the Read command packet and then subtracting 1.

If the byte count is greater than the actual record length, the beginning of the data buffer (lowest addresses) does not contain the data from the tape. Similarly, if the actual record is longer than the byte count, the first part of the record (that nearest to the BOT marker) is not placed in the data buffer.

For any data transfer operation, the Swap Bytes (SWB) bit in the header word of the Read command packet controls the storing of bytes in CPU memory (see Figures 6-2 and 6-3).

6.3.4.3 Set Characteristics Command

The contents of the Set Characteristics command packet tell the subsystem the size of the message buffer and where it is located in memory. The message buffer must be at least seven contiguous words long (or eight, when the extended features provision is enabled), and it must be located on a modulo-4 boundary. The Set Characteristics command packet and characteristics data format are shown in Figure 6-6.

If a correct message buffer address has not been loaded with the Set Characteristics command, the Need Buffer Address (NBA) bit in the TSSR is set.

The Set Characteristics command also transfers a Characteristics Mode byte to the subsystem. This byte, which is the low-order byte in the fourth word of the Characteristics Data Packet, causes specific

actions for certain operational modes. The meaningful bits in the Characteristics Mode byte are defined in the following paragraphs.

Enable Skip Tape Marks Stop (ESS) - Bit 07

When set, ESS instructs the tape transport to stop when a double file mark (two contiguous file marks) is detected during execution of a Skip Tape Marks command. In the default reset state (logic 0), the Skip Tape Marks command terminates only when the file mark count is exhausted or when the BOT marker is sensed by the tape transport.

Enable Tape Mark Stop Off BOT (ENB) - Bit 06

This bit has meaning only when the ESS bit is set. When both ESS and ENB are set (each returns a logic 1 when read), the tape position is at the BOT marker, a Skip Tape Marks Forward command is issued, and the first record encountered is a file mark, then the TC03 subsystem stops the operation and sets the LET status bit (XST0 bit 13). If the ENB bit is clear under these conditions, the subsystem merely counts the file mark and continues the operation.

COMMAND PACKET

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEVICE DEP.			MODE CODE				FORMAT #1			COMMAND CODE				
ACK	CVC	0	0	0	0	0	0	IE	0	0	0	0	1	0	0
A15	LOW-ORDER CHARACTERISTICS DATA ADDRESS														A00
0	HIGH-ORDER CHARACTERISTICS DATA ADDRESS												0	A17	A16
BUFFER EXTENT (BYTE COUNT) (16-BIT POSITIVE INTEGER)															

MODE: 0000 = Load message buffer address and set device characteristics

CHARACTERISTICS DATA

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
A15	LOW-ORDER MESSAGE BUFFER ADDRESS														A00
0	HIGH-ORDER MESSAGE BUFFER ADDRESS												0	A17	A16
LENGTH OF MESSAGE BUFFER (AT LEAST 14 BYTES LONG) (16-BIT POSITIVE INTEGER)															
0	0	0	0	0	0	0	0	CHARACTERISTIC MODE BYTE ESS	ENB	EAI	ERI	0	0	0	0

Figure 6-6. Set Characteristics Command Packet and Characteristics Data Format

Enable Attention Interrupts (EAI) - Bit 05

When this bit is cleared, Attention conditions (such as transitions from Online mode to Offline mode) and microdiagnostic failures do not result in ATTN interrupt messages being sent to the CPU. Instead, the Attention condition is not noticed until the next command is issued, and that next command is rejected.

When this bit state is set to logic 1, Attention conditions cause an ATTN message to be generated (and an interrupt to be sent to the CPU if the IE bit was set on the last command) as soon as the TC03 subsystem owns control of the message buffer.

Enable Message Buffer Release Interrupts (ERI) - Bit 04

If the state of this bit is logic 0, interrupts are not generated upon completion of a Message Buffer Release command. Upon recognition of the command, only the Subsystem Ready (SSR) status bit in the TSSR is reasserted. If the ERI bit is set to return a logic 1 when read, an interrupt is generated (without an accompanying message packet).

Remote Density Select (RDS) - Bit 00

When RDS is set, the subsystem selects NRZI format; when this bit is cleared, it selects PE format. This bit is meaningful only when the tape is positioned at the BOT marker, switch SW1-3 is ON, and SW2-9 is OFF (see also subsection 4.3.5.4).

6.3.4.4 Write Command

Write operations can be performed in either of two normal modes: Write Data or Write Data Retry. Each write operation transfers data onto the tape in the forward direction only. Allowable mode codes for these functions are written in the header word of the Write command packet, and are listed in the following table:

Mode	Function
0000	Write Data
0010	Write Data Retry (Space Reverse, Erase, then Write Data)

Words, fields, and bits in the Write command packet are shown in Figure 6-7.

The Write command packet contains four words:

- A header word
- Two words that specify the address of the data buffer in the CPU memory space where the data to be written onto tape are stored

- A Buffer Extent (byte count) word that specifies the number of bytes available in the data buffer and the number of bytes to be written onto tape

A byte count of 0 specifies that 65,536 (64K) bytes are to be written.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEVICE DEP.			MODE CODE				FORMAT #1			COMMAND CODE				
ACK	CVC	0	SWB	X	X	X	X	IE	0	0	0	0	1	0	1
A15	LOW ORDER BUFFER ADDRESS														A00
0	HIGH ORDER BUFFER ADDRESS									A21	A20	A19	A18	A17	A16
BUFFER EXTENT (BYTE COUNT) (16-BIT POSITIVE INTEGER)															

MODE: 0000 = Write Data
0010 = Write Data Retry (Space Reverse, Erase, Write Data)

Figure 6-7. Write Command Packet

NOTE

Bits <A21:A18> are used only when 22-bit addressing is enabled (see subsection 4.4.5.2).

If execution of a Write command is attempted at or beyond the EOT marker, a Tape Status Alert (TSA) termination occurs (see Table 6-1, TC2). The EOT status bit remains set until the EOT marker is passed while the tape is moving in the reverse direction, or until the subsystem is initialized.

If execution of a Write command is attempted anywhere on the tape and the Identification Burst (IDB) was previously written incorrectly or was not found when the tape position left the BOT, the Density Check (DCK) bit (XST3, bit 03) is set and a Tape Position Lost (TC6) termination occurs.

For any of the Write modes, the Swap Bytes (SWB) bit, in the header word of the Write command packet, controls fetching of bytes from CPU memory (see Figures 6-2 and 6-3).

6.3.4.5 Position Command

The Position command can cause the tape to space records forward or reverse; to skip file marks forward or reverse; or to rewind to the BOT marker.

The mode code bits in the header word of the Position command packet define the positioning function to be performed. For a Rewind command, the Tape Mark/Record Count in the second word of the Position command packet is ignored. The mode codes are listed and defined in the following table:

Mode	Function
0000	Space Records Forward
0001	Space Records Reverse
0010	Skip Tape Marks Forward
0011	Skip Tape Marks Reverse
0100	Rewind (Tape Mark/Record Count ignored)

Words, fields, and bits in the Position command packet are shown in Figure 6-8.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEVICE DEP.			MODE CODE				FORMAT #1			COMMAND CODE				
ACK	CVC	0	0	X	X	X	X	IE	0	0	0	1	0	0	0
TAPE MARK/RECORD COUNT (16-BIT POSITIVE INTEGER)															

Figure 6-8. Position Command Packet

The Space Records operation skips over the number of records specified in the Record Count word of the Position command packet, but the operation automatically terminates with a TSA code if a file mark is encountered during execution of the operation. (The file mark is included in the Record Count.) Also, if the record count is not decremented to 0, the RLS error bit (XST0 bit 14) is set.

The Skip Tape Marks operation skips over the number of file marks specified in the Tape Mark Count word of the Position command packet, but the operation is automatically terminated if two contiguous file marks without intervening data are encountered while the ESS bit in the Characteristics Mode Byte is set (as a result of the last Set Characteristics command packet).

Termination of a Skip Tape Marks command can also occur if a file mark is the first record read after leaving the BOT marker when the ESS and ENB bits in the Characteristics Mode Byte are set (as a result of the last Set Characteristics command packet). Also, if the record count is not decremented to 0, the RLS error bit (XST0 bit 14) is set.

During command execution, any Space Records Reverse or Skip Tape Marks Reverse operation that encounters the BOT marker sets the Reverse Into BOT (RIB) error status bit (XST3 bit 00) and causes a TSA termination. If one of these reverse-motion commands is issued while the tape is already positioned at the BOT marker, the Nonexecutable Function (NEF) error status bit (XST0 bit 10) is set and a Function Reject termination occurs (see Table 6-1, TC3). When the NEF error status bit is set, the tape is prevented from moving.

If the DCK error is present when a Position command is issued, the DCK error status bit (XST3 bit 03) is set, but the operation is not stopped. The Positioning operation is terminated with a TSA termination. This function restriction allows tapes with a bad Identification Burst (IDB) area to be read.

When a Rewind command is issued, the interrupt (if enabled) does not occur until the tape reaches the BOT marker and has stopped.

NOTE

If the tape is positioned between BOT and the first record when a Space Reverse or Skip Reverse command is issued, the RIB error status bit is set and the contents of the Residual Frame Count Register (RBPCR) is the same as the specified record count in the Positioning command.

6.3.4.6 Format Command

The Format command can be used to write a file mark, rewrite a file mark, or erase the tape. The mode code bits in the header word of the Format command packet define the function to be performed. The mode codes are listed and defined in the following table:

Mode	Function
0000	Write Tape Mark
0001	Erase
0010	Write Tape Mark Retry (Space Reverse, Erase, Write Tape Mark)

Words, fields, and bits in the Format command packet are shown in Figure 6-9.

NOTE

Although the second word is present (fetched by the TC03 subsystem), it is not used in the Format command, and the state of each bit in this word should be logic 0.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEVICE DEP.			MODE CODE				FORMAT #1			COMMAND CODE				
ACK	CVC	0	0	X	X	X	X	IE	0	0	0	1	0	0	1
NOT USED															

Figure 6-9. Format Command Packet

In all operations, attempting to execute a Format command at or beyond the EOT marker causes a TSA termination. Error status bit EOT (XST0 bit 00) is set, and it remains set until the EOT marker is passed while the tape is moving in the reverse direction.

The Write Tape Mark command causes approximately 3.75 inches of tape to be erased and a file mark to be written. The Erase command merely causes 3.75 inches of tape to be erased. Successive Erase commands can be used to erase more than 3.75 inches of tape, but only in 3.75-inch increments. The erase length is controlled automatically by tape transport hardware.

The Write Tape Mark Retry command causes a Space Reverse operation (over the previous record), followed by an erase of 3.75 inches of tape, followed by a Write Tape Mark operation (which erases another 3.75-inch segment of tape before writing the new file mark). If the tape is at the BOT position when the Write Tape Mark Retry command is issued, the attempted operation is aborted with a Function Reject termination (TC3), and error status bit NEF (XST0 bit 10) is set.

Any attempt to execute a Format command while error status bit DCK (XST3 bit 03) is set causes a Tape Position Lost termination (TC6).

6.3.4.7 Control Command

The Control command packet can be used to point to three Normal command modes: Message Buffer Release, Unload, and Clean Tape.

The mode code bits in the header word of the Control command packet define the function to be performed. The mode codes are listed and defined in the following table:

Mode	Function
0000	Message Buffer Release
0001	Unload
0010	Clean Tape

Words, fields, and bits in the Control command packet are shown in Figure 6-10.

NOTE

Although the second word is present (fetched by the TC03 subsystem), it is not used in the Control command, and the state of each bit in this word should be logic 0.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEVICE DEP.			MODE CODE				FORMAT #1			COMMAND CODE				
ACK	CVC	0	0	X	X	X	X	IE	0	0	0	1	0	1	0
NOT USED															

Figure 6-10. Control Command Packet

When the Message Buffer Release command is executed with the ACK bit set, ownership of the message buffer is passed to the subsystem, so that it can update the status area in the message buffer in response to an ATTN condition. This function is beneficial when the operating system is processing data in other areas that are not related to the TC03 subsystem and the host CPU needs information about the current status of the subsystem.

The Unload command is used to rewind the tape completely onto the supply reel and place the tape transport in the Offline mode. When this command is executed, termination occurs immediately, and an interrupt message is sent to the CPU if the IE bit has been set in the header word of the Control command packet.

The Clean Tape command moves 10 inches of tape over the tape cleaners on the tape transport and then returns the tape to the original position. Successive Clean Tape commands are not recommended, because they may cause the tape to creep outside the margins of the inter-record gap (IRG). Also, the Clean Tape command does not recognize BOT; therefore, tape can be cleaned while reversing past the BOT marker and then moving forward again without setting any status bits.

6.3.4.8 Initialize Command

If there are no microdiagnostic errors, this command is treated as a No-Op command and results in a message buffer update, just as the update is performed in a Get Status command. If errors are present, however, this command performs the same functions as a Write operation into the TSSR. The Initialize command is not very useful, but it is included for compatibility with command packet protocol.

In the header word of the Initialize command packet there is only one mode code available, 0000. Therefore, all bits in the mode code field are cleared and return a logic 0 when read. Words, fields, and bits in the Initialize command packet are shown in Figure 6-11.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEVICE DEP.			MODE CODE				FORMAT #1			COMMAND CODE				
ACK	CVC	0	0	0	0	0	0	IE	0	0	0	1	0	1	1
NOT USED															

Figure 6-11. Initialize Command Packet

NOTE

Although the second word is present (fetched by the TC03 subsystem), it is not used in the Initialize command, and the state of each bit in this word should be logic 0.

6.3.5 MESSAGE PACKET HEADER WORD

Words, fields, and bits in the message packet header word are shown in Figure 6-12, and the bit functions are explained in the following paragraphs.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	RESERVED			CLASS CODE				PACKET FORMAT #1			MESSAGE CODE				
ACK	0	0	0	0	0	C	C	0	0	0	1	M	M	M	M

Figure 6-12. Message Packet Header Word

Acknowledge (ACK) - Bit 15

This bit is used by the TC03 subsystem to inform the CPU that the command buffer is available for any pending or subsequent command packets. This bit is not set for an ATTN message, because the subsystem does not own the command buffer.

Reserved - Bits <14:12>

These bits are reserved for future expansion and should always return logic 0 when read.

Class Code Field - Bits <11:08>

These bits define the class of message in the remainder of the message buffer. Class codes are defined as listed in the following table.

Message Type	Class Value	Definition
ATTN	0000	Online or Offline status
FAIL	0001	Other (ILC, ILA, NBA)
FAIL	0010	Write Lock Error (WLE) or Non-Executable Function (NEF)

Packet Format #1 Field - Bits <07:05>

Only a single value for this field is supported by the TC03: 000, meaning One Word Header.

Message Code - Bits <04:00>

The bits in this field indicate the definition codes listed in the following table.

Termination Class	Value	Definition
0 and 2	10000	End
3	10001	Fail
4, 5, 6, and 7	10010	Error
1	10011	Attention

6.3.5.1 Message Packet Example

All message packets are identical. Each contains the message packet header word, the data length word from the RBPCR, and the contents of four extended status registers (XST0, XST1, XST2, and XST3), as shown in Figure 6-13.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEVICE STATUS			STANDARD STATUS				PACKET FORMAT #1			MESSAGE CODE				
ACK	0	0	0	0	0	X	X	0	0	0	M	M	M	M	M
0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
RBPCR															
XST0															
XST1															
XST2															
XST3															

MESSAGE CODE:
BITS <04:00>

10000 = END
10001 = FAIL
10010 = ERROR
10011 = ATTN

STANDARD STATUS:
BITS <11:08>

FAIL MESSAGE
0001 = OTHER
0010 = WRITE LOCK ERROR (WLE) OR NON-EXECUTABLE FUNCTION (NEF)

ATTN MESSAGE
0000 = ONLINE MODE OR OFFLINE MODE TRANSITION

Figure 6-13. Message Packet Example

6.4 PROGRAMMING OPERATIONS

This subsection explains four major requirements for operating and programming the tape transport subsystem:

- LSI-11 bus registers
- Command packets and message packets
- Special conditions and errors
- Status error handling techniques

6.4.1 LSI-11 BUS REGISTERS

The subsystem has two LSI-11 bus word locations that are used to access device registers: the base address and the base address plus 2. When written to, the base address is the LSI-11 Bus Data Buffer (TSDB); when read, it is the LSI-11 Bus Address Register (TSBA). The second device register (base address plus 2) is the Status Register (TSSR). Writing to the TSSR causes a subsystem Initialize command to be executed, and reading from the TSSR contents provides the CPU with device status information. See subsections 6.2.1 and 6.2.3 for information regarding the TSBA, TSDB, and TSSR registers.

The TSDB is the only register that is written to during normal operations. DATO, or word access, must be used to write command pointers properly into the TSDB. DATOB, or byte access to the TSDB, causes maintenance functions to be performed.

Commands are not written to the subsystem's LSI-11 bus registers. Instead, command pointers, which point to a command packet somewhere in CPU memory space, are written to the TSDB to initiate a command. The command pointer is used by the subsystem to retrieve the words in the command packet, which instruct the subsystem to perform a given function. The words in the command packet also contain any function parameters, such as bus address, byte count, record count, and modifier flags.

6.4.2 COMMAND PACKETS AND MESSAGE PACKETS

Command packets must reside on modulo-4 address boundaries within CPU memory space. In other words, the starting address of the command packet must be divisible by four: 00_8, 04_8, 10_8, 14_8, and so on.

All four words of a command packet must exist and have proper memory parity, even if all four words are not used by a command. For instance, the Rewind command uses only one word.

Message packets are issued by the subsystem and are deposited in CPU memory. Controlled operation of the subsystem requires that it be supplied with a message buffer address from a Set Characteristics command. The contents of the five extended status registers are stored in this message buffer area. The END message packet, which is sent when execution of any command is done, contains these extended status words.

6.4.3 SPECIAL CONDITIONS AND ERRORS

The termination class code field in the TSSR contains termination class codes in binary format. These binary values are listed and described in Table 6-1.

6.4.4 STATUS ERROR HANDLING TECHNIQUES

In the TSSR, the SC bit and error bits other than the fatal termination class (TC7) are cleared by loading a command pointer into the TSDB. The SC bit is reset if it was set by set UPE, SPE, RMR, or NXM error bits in the TSSR. Extended status error bits are cleared after the END message packet is sent.

All commands (even the Get Status command) clear all error bits in the extended status registers, except XST3 bits <15:08> and 01.

Normally, the TC03 does not respond to a new command for the selected tape transport while another command execution is in progress on that tape transport. If an attempt is made to issue a new command while another command is being executed, the RMR error status bit (TSSR bit 12) is set, unless one of the following exceptions exists:

- A DATO (word access) to the TSSR (subsystem Initialize operation) brings any operation in progress to an immediate halt. All subsystem parameters that were in the memory of the subsystem (VCK reset, EOT, etc.) are erased.
- The subsystem responds to any non-tape motion command while performing a Rewind and Unload operation (while the tape transport is in the Offline mode), because the SSR status bit (TSSR bit 07) is still set.

The subsystem also responds to any commands that do not require tape motion (Get Status, Initialize, Set Characteristics, and Message Buffer Release) when offline, except when in the Maintenance mode. In the Maintenance mode, SSR is not asserted, so commands that do not require tape motion cause setting of the RMR bit.

If a command packet header word has the Interrupt Enable (IE) bit set (bit 07), a failure condition normally results in an Interrupt, but certain failures can occur with IE set without resulting in an Interrupt. Such failures are identified by the set condition of the error status bits NXM and UPE. These error status bits may be set before the IE bit is fetched as part of the command packet.

BLANK

7.1 OVERVIEW

This section contains a description of the TC03 Tape Coupler's architecture. The following table outlines the contents of this section.

Subsection	Title
7.1	Overview
7.2	TC03 Tape Coupler Architecture
7.3	Tape Format

7.2 TC03 TAPE COUPLER ARCHITECTURE

7.2.1 ORGANIZATION

Figure 7-1 is a block diagram that shows the functional relation of major components. The TC03 Tape Coupler is organized around an eight-bit, high-speed, bipolar microprocessor. The ALU and register file portion of the microprocessor are implemented with two AMD 2901 bit-slice components. The micro-instruction is 48 bits long, and the control memory of 2K words is implemented with six 2K x 8-bit PROM ICs.

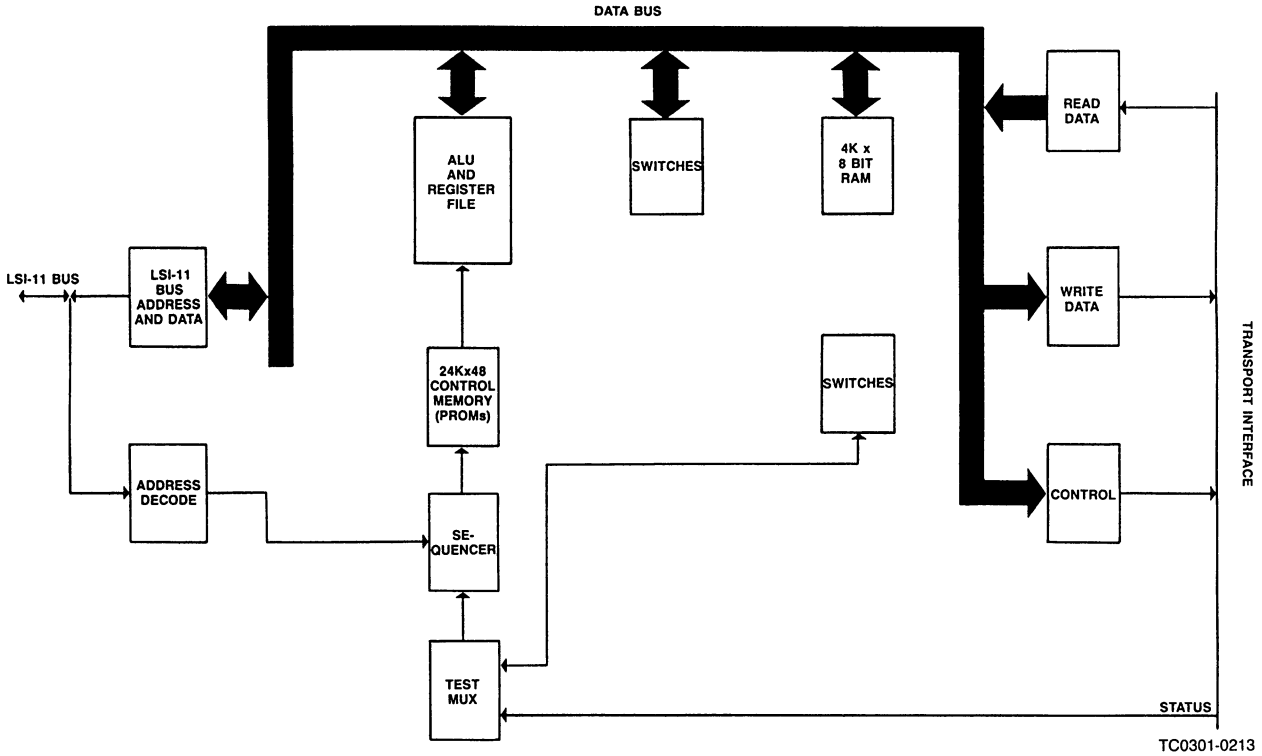


Figure 7-1. TC03 Tape Coupler Block Diagram

7.2.2 RAM BUFFER

All the device registers of the TC03 Tape Coupler, the 3584-word data buffer, and working storage are contained in a 4K x 8-bit random access memory (RAM) buffer.

7.2.3 DATA AND CONTROL REGISTERS

The data and control registers described in this subsection are internal registers that are not visible to the LSI-11 bus.

The Write Data Register (WDR) holds the nine bits of data to be transferred to the tape transport, and the Read Data Register (RDR) receives the nine data bits from the tape transport. The Control Register latches internal microprocessor control signals, as well as the external signals that are used to control the tape transport. The status signals from the tape transport are testable signals to the microprocessor.

7.2.4 MICROPROCESSOR RELATIONSHIPS

The microprocessor responds to all programmed input/output (I/O) and carries out the I/O functions required for the addressed register in the TC03 Tape Coupler. The microprocessor also controls all NPR operations and transfers data between the LSI-11 bus data lines and the tape cartridge subsystem via its own internal buffer.

For a description of the LSI-11 bus interface and tape transport interface, see Section 8.

7.3 TAPE FORMAT

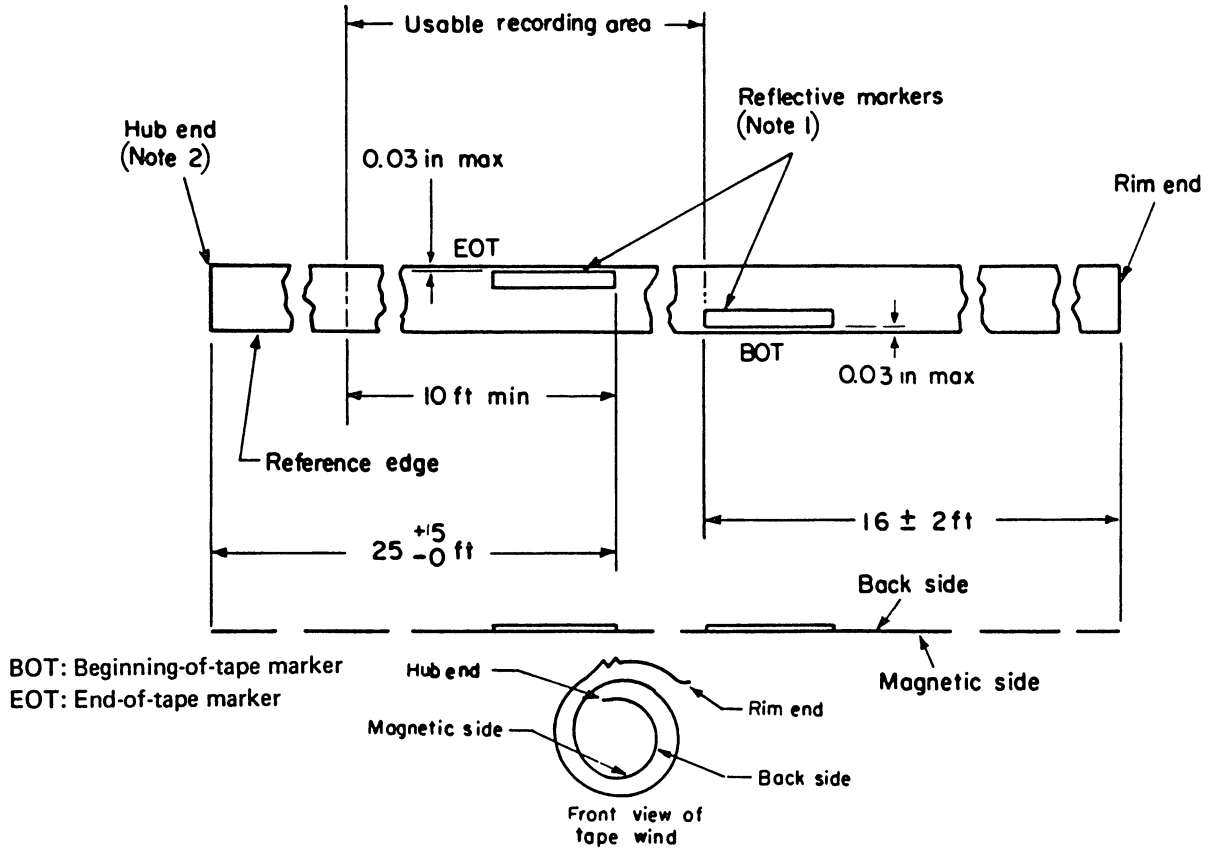
The TC03 can be used with tape transports that use NRZI, PE, or GCR formats.

7.3.1 NRZI FORMAT

The NRZI format supported by the TC03 tape coupler is the 800 cpi NRZI format specified in the American National Standards Institute (ANSI) Standard X3.22-1973.

The usable recording area of the NRZI format is shown in Figure 7-2, and the NRZI recording format is shown in Figure 7-3.

AMERICAN NATIONAL STANDARD X3.22-1973



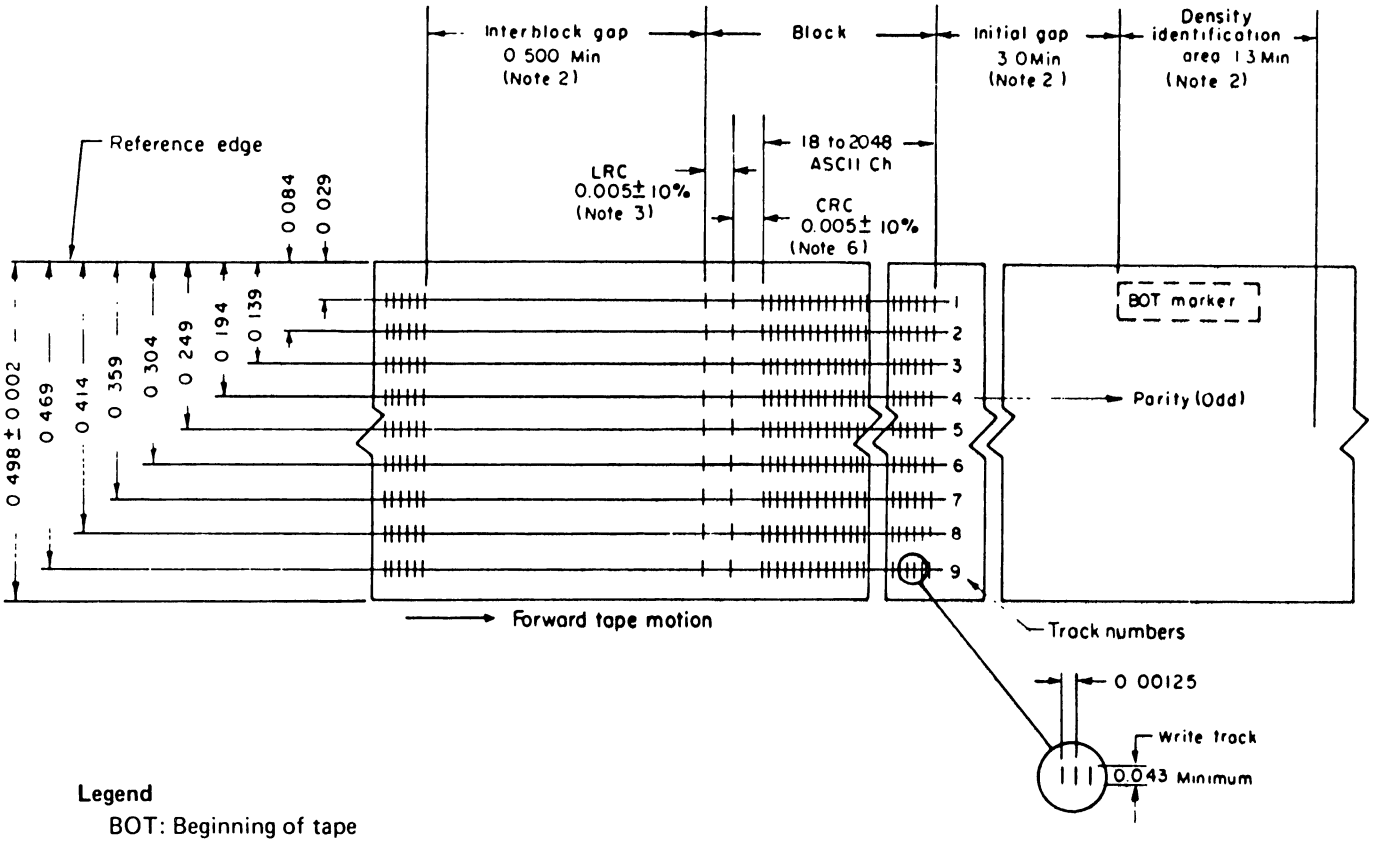
NOTES:

(1) Photoreflective markers shall not protrude beyond the edge of the tape and shall be free of wrinkles and excessive adhesive. Marker dimensions: length, 1.1 inch ± 0.2 inch; width, 0.19 inch ± 0.02 inch; thickness, 0.0008 inch maximum.

(2) Tape shall not be attached to the hub.

TC0301-0258

Figure 7-2. Usable Recording Area in 800 cpi NRZI Format



Legend

BOT: Beginning of tape
Ch: Characters
CPI: Characters per inch
CRC: Cyclic redundancy check
LRC: Longitudinal redundancy check
Min: Minimum

NOTES:

(1) Tape is shown with oxide side up, Read/Write head on same side as oxide.
(2) Tape to be fully saturated in the erased direction in the interblock gap, the initial gap, and density identification area.
(3) A longitudinal redundancy check bit is written in any track if the longitudinal count in that track is odd. Character parity is ignored in the longitudinal redundancy check character.
(4) All dimensions are given in inches.
(5) There is a track placement tolerance of ± 0.003 inch for each track.
(6) Parity of CRC character is odd, if an even number of data characters are written.

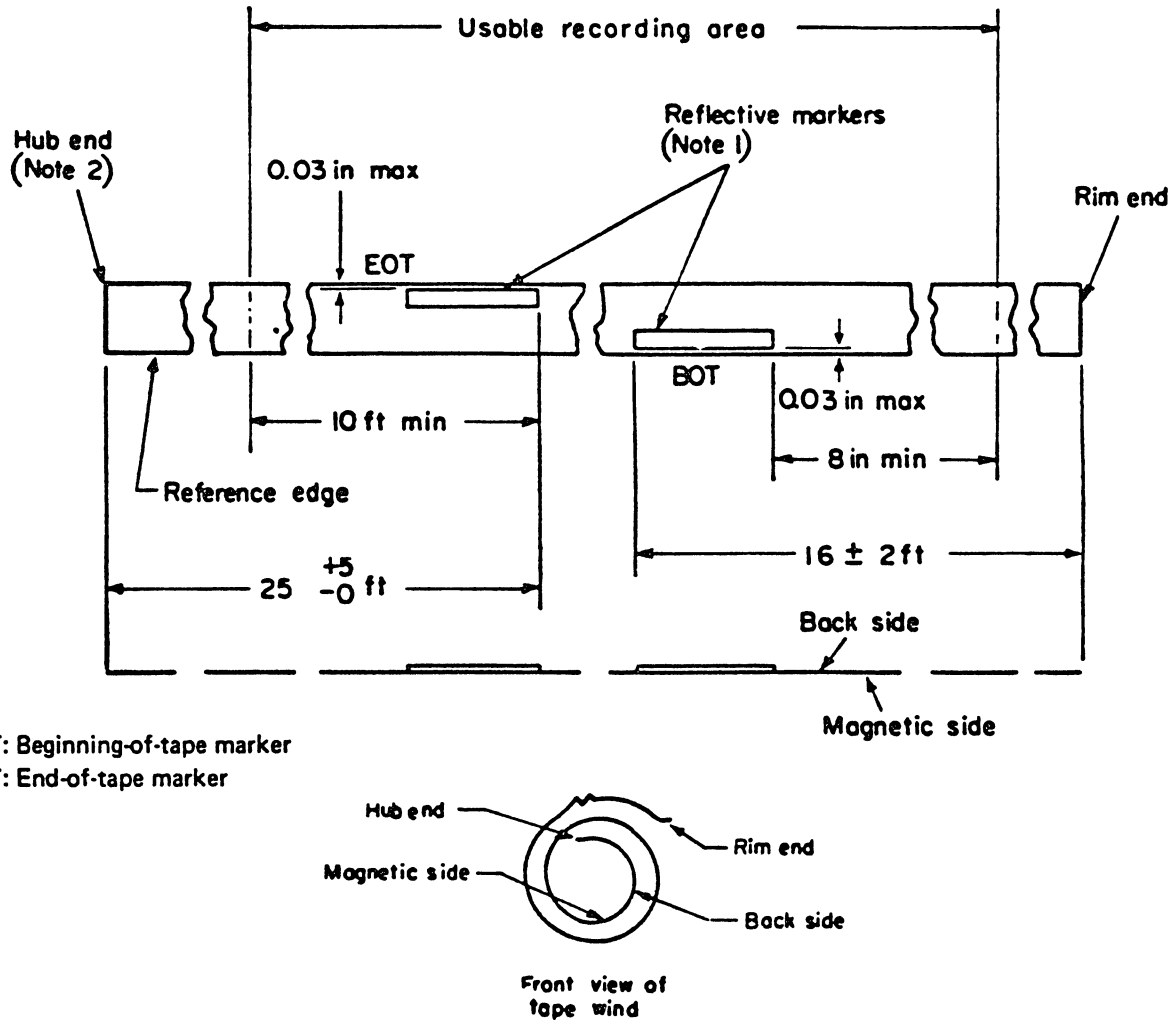
TC0301-0259

Figure 7-3. NRZI Recording Format

7.3.2 PE FORMAT

The PE format supported by the TC03 tape coupler is the 1600 cpi PE format specified in ANSI Standard X3.39-1973.

The usable recording area of the PE format is shown in Figure 7-4, and the PE recording format is shown in Figure 7-5.



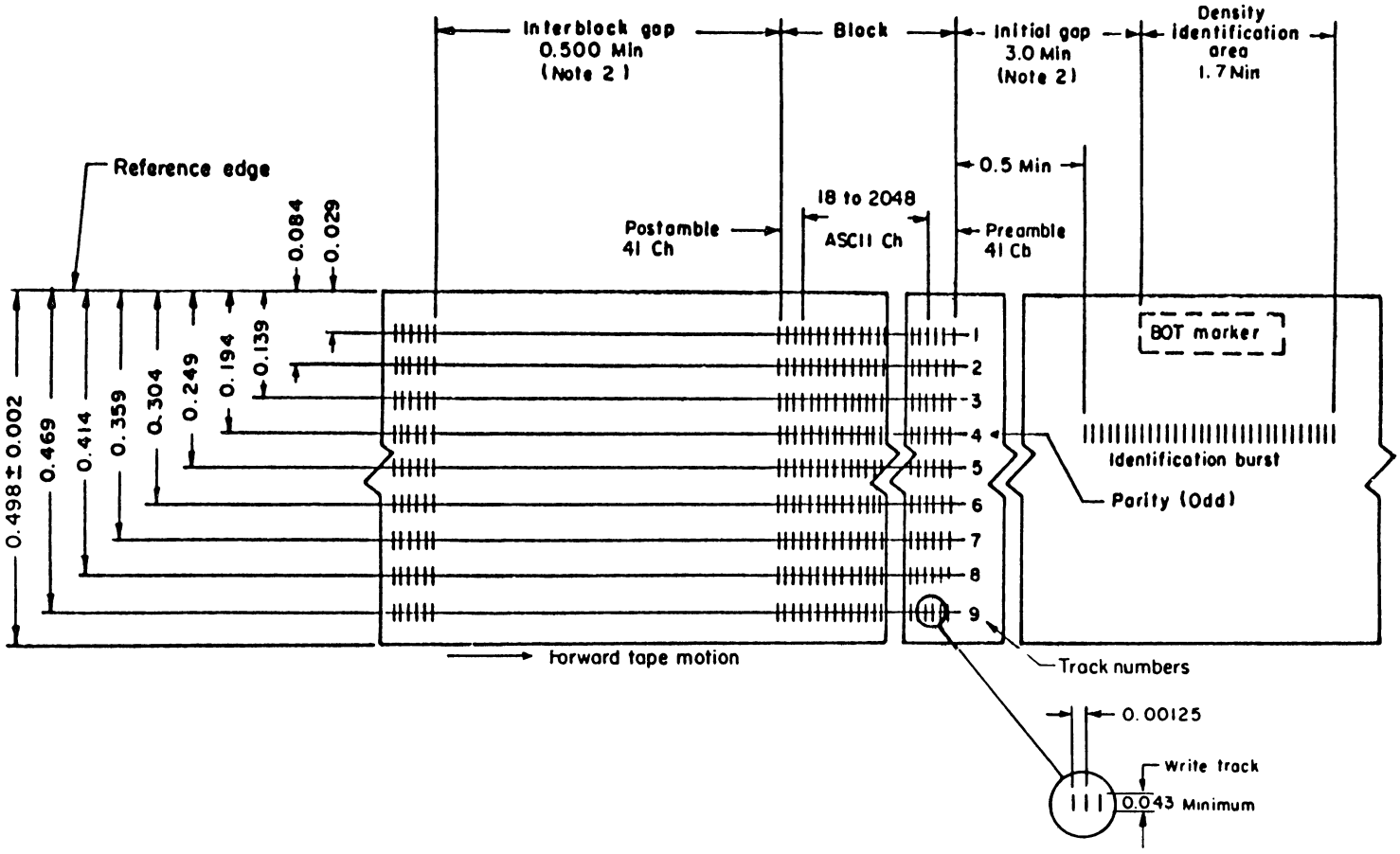
NOTES:

(1) Photoreflective markers shall not protrude beyond the edge of the tape and shall be free of wrinkles and excessive adhesive. Marker dimensions: length, 1.1 inch ± 0.2 inch; width, 0.19 inch ± 0.02 inch; thickness, 0.0008 inch maximum.

(2) Tape shall not be attached to the hub.

TC0301-0260

Figure 7-4. Usable Recording Area in 1600 cpi PE Format



Legend

BOT: Beginning of tape
Ch: Characters
CPI: Characters per inch
Min: Minimum

NOTES:

(1) Tape is shown with oxide side up, Read/Write head on same side as oxide.
(2) Tape to be fully saturated in the erased direction in the interblock gap and the initial gap.
(3) The identification burst extends past the trailing edge of the BOT marker.
(4) All dimensions are given in inches.
(5) There is a track placement tolerance of ± 0.003 inch for each track.

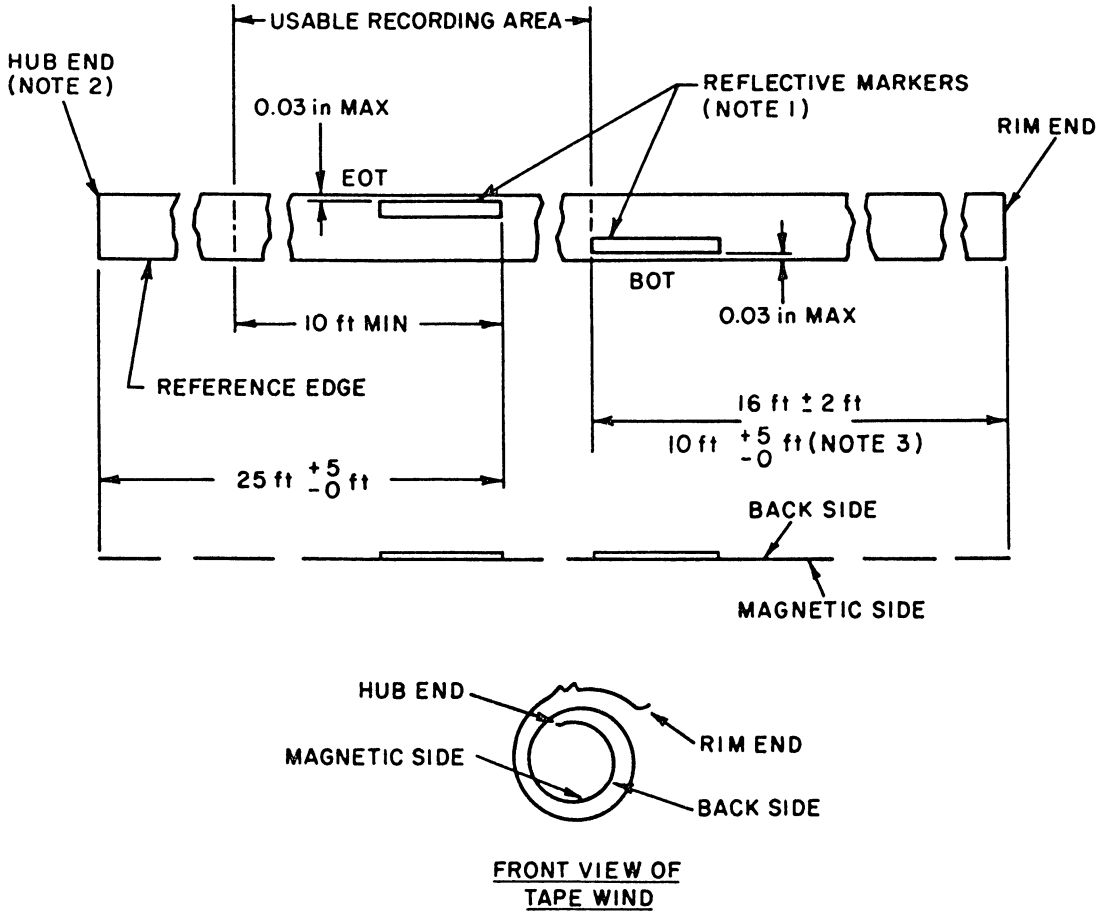
TC0301-0261

Figure 7-5. PE Recording Format

7.3.3 GCR FORMAT

The GCR format supported by the TC03 tape coupler is the 6250 cpi GCR format specified in ANSI Standard X3.54-1976.

Figure 7-6 shows the usable recording area of the GCR format. The GCR recording format is shown in Figure 7-7, and the group organization of the GCR format is shown in Figure 7-8.



Legend

BOT: Beginning-of-tape marker

EOT: End-of-tape marker

NOTES:

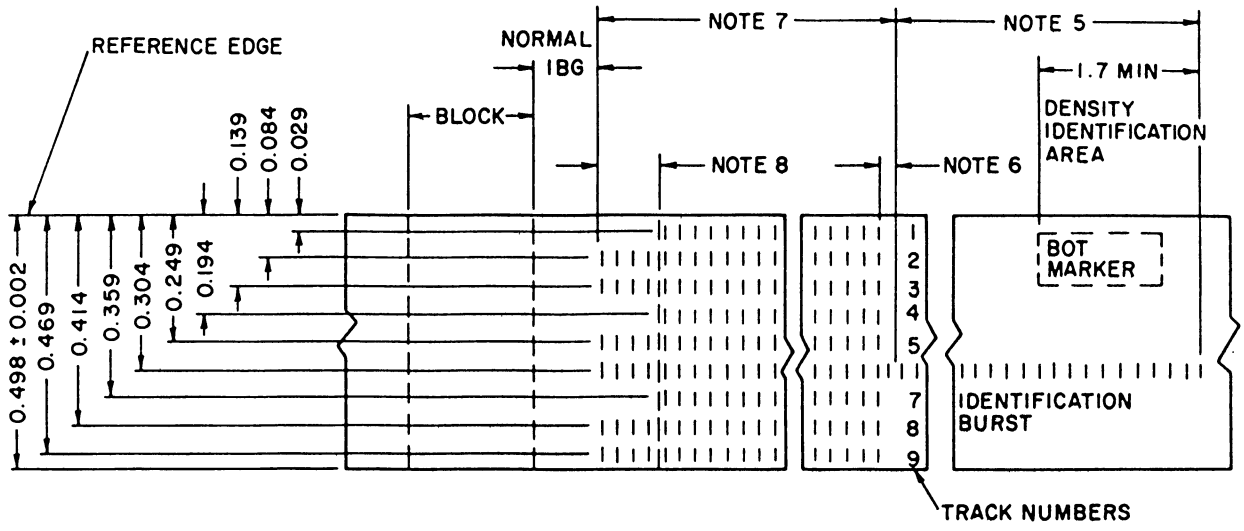
(1) Photoreflective markers shall not protrude beyond the edge of the tape and shall be free of wrinkles and excessive adhesive. Marker dimensions: length, 1.1 inch ± 0.2 inch; width, 0.19 inch ± 0.02 inch; thickness, 0.0008 inch maximum.

(2) Tape shall not be attached to the hub.

(3) Two values for placement of the BOT marker are given, both of which can be handled by most tape units. The indicated value of 16 feet ± 2 feet is the current specified dimension.

TC0301-0262

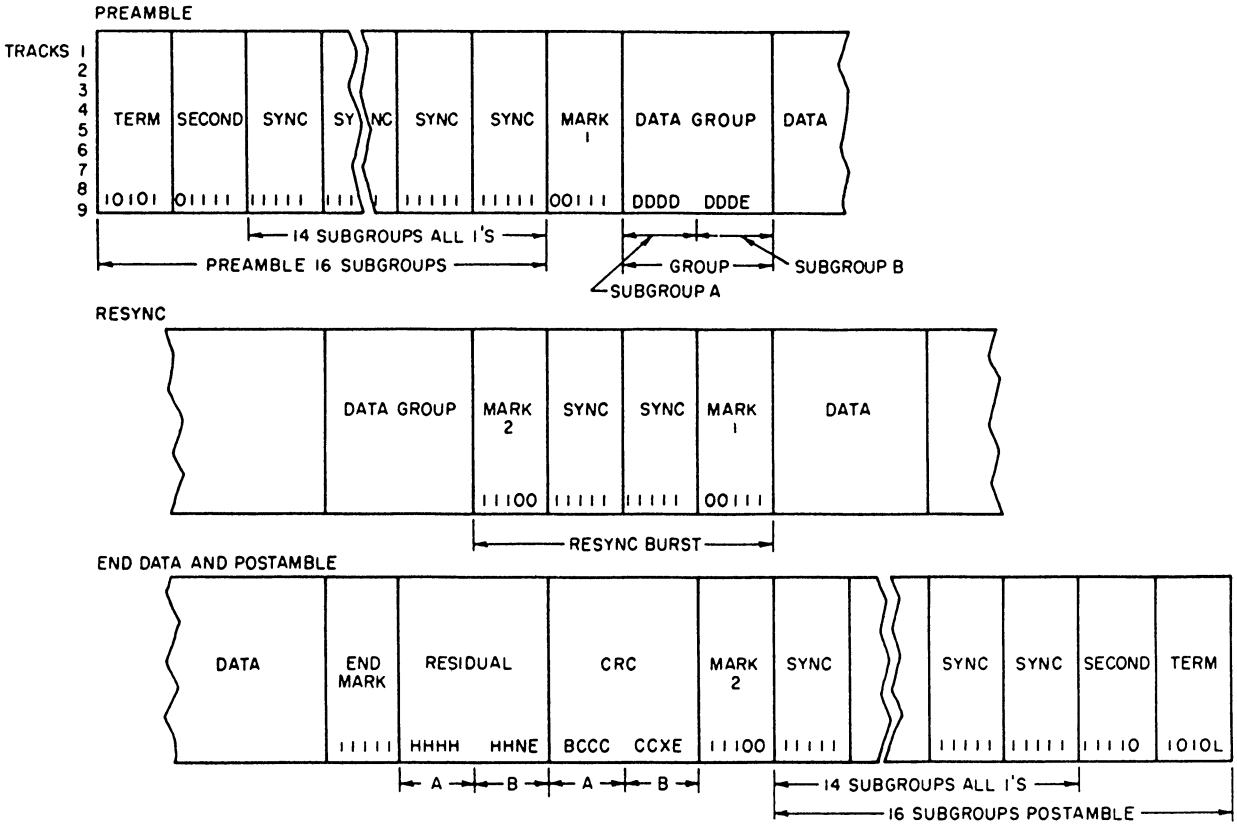
Figure 7-6. Usable Recording Area in 6250 cpi GCR Format



NOTES:
(1) Tape is shown in 6250 mode, oxide side up.
(2) All dimensions are given in inches.
(3) Track placement tolerance is ± 0.003 for each track.
(4) Tape to be fully saturated in the erase direction in the interblock gap and the ID area.

TC0301-0263

Figure 7-7. GCR Recording Format



Legend:

D: Data characters	C: CRC character
H: Pad or data character	N: Auxiliary CRC character
X: Residual character	L: Last character
E: ECC character	B: CRC or pad character

NOTE: This figure portrays the format prior to the encoding of the data, residual, and CRC groups in accordance with Table 2. The control subgroups are recorded on tape as shown and described.

TC0301-0264

Figure 7-8. Group Organization of GCR Recording Format

Section 8
INTERFACES

8.1 OVERVIEW

This section contains a detailed description of controller interfaces used with the TC03 coupler. It is divided into three subsections:

Subsection	Title
8.1	Overview
8.2	LSI-11 Bus Interface
8.3	Tape Transport Interface

The PCBA is designed to interface with connector rows A, B, C, and D on the LSI-11 CPU backplane. The 18 pins in each connector row are reference designated A through V, except that letters G, I, O, and Q (from right to left) are not used. In designations of pin/signal assignments, the component side of the PCBA is side 1 and the solder side is side 2.

NOTE

In this manual, directions for locating components on the PCBA assume that the TC03 is being viewed from the component side with edge connectors A, B, C, and D at the bottom.

The TC03 tape coupler interfaces with the tape transport via two 50-pin connectors, reference designated J1 and J2. These connectors are located next to the top edge of the PCBA. Two additional male connectors, reference designated J3 and J4, are also included on the PCBA. Connector J3 is in the upper left corner of the PCBA, and connector J4 is in the upper right corner. Connectors J3 and J4 enable a special test panel to be connected for factory test and repair operations. They are not intended for use in normal operations of the TC03 Tape Coupler.

8.2 LSI-11 BUS INTERFACE

The LSI-11 bus between the LSI-11 CPU and the TC03 Tape Coupler contains 42 bidirectional signal lines and two unidirectional signal lines on connectors A and B, and two unidirectional signal lines on connector C. LSI-11 bus interface pin assignments are listed and described in Table 8-1. These signal lines provide the means by which the LSI-11 CPU and the TC03 Tape Coupler communicate with each other.

The LSI-11 bus interface is used for programmed I/O, CPU interrupts, and NPR data transfer operations. Addresses, data, and control information are sent along these signal lines, some of which contain time-multiplexed information. The LSI-11 bus interface lines are grouped in the following categories:

- Twenty-two data/address lines, <BDAL00:BDAL21>. The four data/address lines that carry the most significant bits (MSB) are lines BDAL21 through BDAL18. They are used for addressing only and do not carry data. Lines BDAL17 and BDAL16 reflect the parity status of the 16-bit data word during a Write or Read Data Transfer operation via the LSI-11 bus cycle.

- Six data transfer control lines: BBS7, BDIN, BDOUT, BRPLY, BSYNC, and BWTBT.

- Six direct memory access (DMA) control lines: BDMR, BSACK, BDMGI, and BDMGO (connectors A and C).

- Seven interrupt control lines: BEVNT, BIAKI, BIAKO, BIRQ4, BIRQ5, BIRQ6, AND BIRQ7.

- Five system control lines: BDCOK, BHALT, BINIT, BPOK, and BREF.

Table 8-1. LSI-11 Bus Interface Pin Assignments

Connector A Signal			Connector B Signal		
Component Side	Pin	Solder Side	Component Side	Pin	Solder Side
BIRQ5	A	+5V	BDCOK	A	+5V
BIRQ6	B		BPOK	B	
BDAL16	C	0V (GND)	BDAL18	C	0V (GND)
BDAL17	D		BDAL19	D	
	E	BDOUT	BDAL20	E	BDAL02
	F	BRPLY	BDAL21	F	BDAL03
	H	BDIN		H	BDAL04
0V (GND)	J	BSYNC	0V (GND)	J	BDAL05
	K	BWTBT		K	BDAL06
	L	BIRQ4		L	BDAL07
0V (GND)	M	BIAKI	0V (GND)	M	BDAL08
BDMR	N	BIAKO	BSACK	N	BDAL09
BHALT	P	BBS7	BIRQ7	P	BDAL10
BREF	R	BDMGI	BEVNT	R	BDAL11
	S	BDMGO		S	BDAL12
0V (GND)	T	BINIT	0V (GND)	T	BDAL13
	U	BDAL00		U	BDAL14
	V	BDAL01		V	BDAL15

Connector C Signal			Connector D Signal		
Component Side	Pin	Solder Side	Component Side	Pin	Solder Side
	A	+5V		A	+5V
	B			B	
	C	0V (GND)		C	0V (GND)
	D			D	
	E			E	
	F			F	
	H			H	
0V (GND)	J		0V (GND)	J	
	K			K	
	L			L	
0V (GND)	M	BIAKI	0V (GND)	M	
	N	BIAKO		N	
	P			P	
	R	BDMGI		R	
	S	BDMGO		S	
0V (GND)	T		0V (GND)	T	
	U			U	
	V			V	

All signals, except BDCOK and BPOK, are low active.

8.2.1 INTERRUPT PRIORITY LEVEL

The TC03 Tape Coupler is hard-wired to issue both level 4 and level 5 interrupt requests. The level 4 request is necessary to allow compatibility with either an LSI-11 or LSI-11/2 CPU.

8.2.2 REGISTER ADDRESS

The register address (1777XXXX) and the eight registers assigned to the TC03 Tape Coupler are decoded by a PROM (reference designated U98). The selections available are determined by configuration DIP switch pack SW1 (see Section 4).

8.2.3 DCOK AND INIT SIGNALS

The DCOK and INIT signals can each perform a Controller Clear operation. The self-test function is performed only when DC power is initially applied (Power-Up mode).

8.2.4 NPR OPERATIONS

All DMA Data Transfer operations are performed under microprocessor control. During a Read from memory operation, a check is made for memory parity errors. If an error is detected, the LSI-11 bus Parity Error (UPE) error status bit is set.

8.3 TAPE TRANSPORT INTERFACE

There is a slight difference in the tape transport interface when the TC03 is functioning with a formatted tape drive rather than a streaming drive. Both interfaces are depicted in Table 8-2. The few pins whose function depends on transport mode have been assigned two mnemonics each: the first mnemonic applies to the streaming tape transport interface and the second to the formatted tape transport interface (HSPD/DEN, for example). The definitions of all signal mnemonics are contained in subsection 8.3.4. Both interfaces are based on the industry-standard Pertec interface.

8.3.1 CONNECTORS AND CABLE

The tape coupler uses two 50-conductor flat cables to interface to the transports. The cable should be a twisted pair with a maximum daisy-chained length of 30 feet. All wires should be 24 AWG minimum, and each pair should have not less than one twist per inch. Connectors are standard 50-pin flat cable connectors.

8.3.2 INPUT CIRCUITS

The input lines from the tape transport are terminated with a 220-ohm (5 percent) resistor to +5 volts (V) and a 330-ohm (5 percent) resistor to ground. All input circuits have maximum low-level input voltage of 0.8 V and minimum high-level input voltage of 2.0 V. The input receivers are all 74LS-type circuits.

8.3.3 OUTPUT CIRCUITS

All output lines must be terminated at the far end of the daisy-chained cable with a 220-ohm (5 percent) resistor to +5 V and a 330-ohm (5 percent) resistor to ground. Output driver circuits are 74LS374 TTL registers, except for some 7438 open collector gates.

8.3.4 SIGNAL DEFINITIONS

8.3.4.1 Coupler to Formatter

- **Transport Address: TAD0, TAD1.** These lines determine which of up to four transports is selected by the coupler. TAD1 is the most significant bit.
- **Formatter Address: FAD.** This signal selects one of two formatters. It is always 0 for this emulation.
- **Initiate Command: GO.** A pulse that initiates any command specified by a combination of the command signals REVERSE, WRT, WFM, ERASE, EDIT, LGAP, and/or HSPD.
- **Rewind Command: REWIND.** A low-level pulse of approximately 1 microsecond (usec) commands the selected transport to rewind to the load point.
- **Unload Command: UNL.** A low-level pulse of approximately 1 usec causes the selected tape transport to go offline, rewind the tape, and when BOT is encountered, unload the tape onto the supply reel.
- **Write: WRT.** Write mode is specified when this signal is TRUE; read mode is specified when it is FALSE.
- **Write File Mark: WFM.** When this signal and WRT are TRUE, the transport writes a file mark on the tape.
- **Erase: ERASE.** When ERASE and WRT are TRUE, the transport executes a dummy Write command. The transport goes through all the operations of a normal Write command, but no data are recorded. A length of tape equivalent to the length of

the dummy record (as defined by LWD) is erased. If ERASE, WRT, and WFM are TRUE, the transport executes a dummy Write File Mark command. A fixed length of tape (approximately 3.75 inches) is erased.

- **High Speed: HSPD.** If this signal is TRUE when a Read or Write command is issued, the transport reads or writes at the high speed.

- **Last Word: LWD.** When TRUE during a Write or Erase command, this signal indicates that the next character to be strobed into the transport (formatter) is the last character of the record.

- **Online: LOL.** This signal causes the selected transport to go online.

- **Reverse: REVERSE.** When TRUE, this signal initiates reverse tape motion. When FALSE, it specifies forward tape motion.

- **Edit: EDIT.** This signal, when TRUE during a read reverse operation, modifies the read reverse stop delay to optimize head positioning for a subsequent edit operation. When EDIT and WRT are TRUE, the selected transport operates in the edit mode.

- **Formatter Enable: FEN.** When FALSE, this signal causes the transport to be held in an initialized state.

- **Write Data 7:0, Parity: WD7:WD0, WDP.** These lines transmit data to the transport. Line 0 is the most significant. WDP carries the odd parity bit associated with each data word. The parity bit is generated by the coupler.

- **Long Gap: LGAP.** When TRUE, this signal causes the transport to generate a 1.2-inch IBG.

- **Read Threshold Level 1: RTH1.** This line is used only by transports with single-gap heads to specify the operating level of the read threshold circuits. A TRUE level specifies selection of the high read threshold level, and a FALSE level specifies the normal read threshold.

- **Read Threshold Level 2: RTH2.** This line is used only by transports with extra low read threshold capabilities. When TRUE, the extra low threshold is specified; when FALSE, the normal threshold is specified.

- **Density: DEN.** When used with a dual-mode transport, the TRUE level selects NRZI and the FALSE level selects PE. When used with tri-density transports, this line selects NRZI/PE, NRZI/GCR, or PE/GCR, depending on transport jumpering.

8.3.4.2 Formatter to Coupler

- **Formatter Busy: FBY.** When TRUE, this signal inhibits further commands to the formatter. The signal becomes TRUE on the trailing edge of GO when a command is issued by the coupler. FBY remains TRUE until a new command can be given.

- **Online: ONL.** A low level indicates that the selected tape transport is online and under control of the tape coupler.

- **Ready: READY.** A low level indicates that the selected tape transport is loaded and not rewinding.

- **Rewinding: RWD.** A low level indicates that the selected tape transport is engaged in a rewind operation or the load sequence following a rewind operation.

- **End of Tape: EOT.** A low level indicates that the EOT tab on the tape is being sensed.

- **Beginning of Tape: BOT.** A low level indicates that the selected tape transport is sensing the BOT tab on the tape and has completed its initial load sequence, and that the tape transport is not rewinding.

- **File Protect: FPT.** A low level indicates that a reel of tape without a write enable ring installed is mounted on the transport.

- **Data Busy: DBY.** This signal becomes TRUE after a command has been accepted by the transport. DBY remains TRUE until the data transfer is complete and the appropriate post-record delay has expired.

- **Hard Error: HER.** A TRUE pulse of this signal indicates that an uncorrectable read error has occurred and that the record should be either reread or rewritten.

- **Corrected Error: CER.** A TRUE pulse of this signal indicates that a single track dropout has been detected and the formatter is performing an error correction.

- **Identification: PEID.** When TRUE, this signal indicates that a PE identification burst has been detected. When in 800 bpi mode (NRZI), this signal is TRUE when the read information being transmitted to the coupler is a cyclic redundancy check character (CRCC) or a longitudinal redundancy check character (LRCC). It is FALSE when data characters are being transmitted.

- **File Mark: FMK.** This signal is pulsed when a file mark is detected on the tape during a read operation, or during a write file mark operation in a read-after-write transport.

- **High Speed Status: HSPS.** When TRUE, this signal indicates that the selected transport is in the 100 ips (streaming) mode. A FALSE level indicates that the transport is operating at low speed (start/stop).

- **NRZI Mode: INRZ.** This signal is TRUE when the transport is in 800 bpi mode (NRZI). Depending on the transport being used, this signal may be used to indicate GCR mode (6250 bpi). See also subsection 4.3.5.4.

Table 8-2. Cable Interface

Connector	Sig Pin	Grd Pin	Mnemonic	Connector	Sig Pin	Grd Pin	Mnemonic
J1	2	1	$\overline{\text{FBY}}$	J2	1	5	$\overline{\text{RDP}}$
	4	3	$\overline{\text{LWD}}$		2	5	$\overline{\text{RD0}}$
	6	5	$\overline{\text{WD4}}$		3	5	$\overline{\text{RD1}}$
	8	7	$\overline{\text{GO}}$		4	5	$\overline{\text{BOT}}$
	10	9	$\overline{\text{WD0}}$		6	5	$\overline{\text{RD4}}$
	12	11	$\overline{\text{WD1}}$		8	7	$\overline{\text{RD7}}$
	14	13	Spare		10	9	$\overline{\text{RD6}}$
	16	15	$\overline{\text{LOL}}$		12	11	$\overline{\text{HER}}$
	18	17	$\overline{\text{REVERSE}}$		14	13	$\overline{\text{FMK}}$
	20	19	$\overline{\text{REWIND}}$		16	15	$\overline{\text{PEID}}$
	22	21	$\overline{\text{WDP}}$		18	17	$\overline{\text{FEN}}$
	24	23	$\overline{\text{WD7}}$		20	19	$\overline{\text{RD5}}$
	26	25	$\overline{\text{WD3}}$		22	21	$\overline{\text{EOT}}$
	28	27	$\overline{\text{WD6}}$		24	23	$\overline{\text{UNL}}$
	30	29	$\overline{\text{WD2}}$		26	25	$\overline{\text{INRZ}}$
	32	31	$\overline{\text{WD5}}$		28	27	$\overline{\text{READY}}$
	34	33	$\overline{\text{WRT}}$		30	29	$\overline{\text{RWD}}$
	36	35	$\overline{\text{LGAP}}/\overline{\text{RTH2}}$		32	31	$\overline{\text{FPT}}$
	38	37	$\overline{\text{EDIT}}^{1}$		34	33	$\overline{\text{RDS}}$
	40	39	$\overline{\text{ERASE}}$		36	35	$\overline{\text{WDS}}$
	42	41	$\overline{\text{WFM}}$		38	37	$\overline{\text{DBY}}$
	44	43	$\overline{\text{RTH1}}$		40	39	$\overline{\text{HSPS}}$
	46	45	$\overline{\text{TAD0}}$		42	41	$\overline{\text{CER}}$
	48	47	$\overline{\text{RD2}}$		44	43	$\overline{\text{ONL}}$
J1	50	49	$\overline{\text{RD3}}$		46	45	$\overline{\text{TAD1}}$
					48	47	$\overline{\text{FAD}}$
				J2	50	49	$\overline{\text{HSPD}}/\overline{\text{DEN}}$

NOTE

In the preceding table, where two mnemonics are given for a pin (HSPD/DEN, for example), the first applies to the streaming tape interface and the second applies to the formatted tape interface.

- **Write Data Strobe: WDS.** This signal is pulsed each time a data character is written onto tape. WDS samples the write data lines WDP, WD7:WD0 from the coupler and copies this information, character by character, into the formatter write logic. The first character should be available prior to the first write strobe pulse, and succeeding characters should be set up within half a character period after the trailing edge of each write strobe.

- **Read Data Strobe: RDS.** This signal consists of a pulse for each character of read information to be transmitted to the coupler. This signal should be used to sample the read data lines RDP, RD7:RD0.

- **Read Data 7:0, Parity: RD7:RD0, RDP.** Each character read from tape is made available by parallel sampling the read lines with RDS. Because the data remains on the read data lines for a full character period, corresponding RDS pulses are timed to occur after approximately the center of the character period.

Appendix A
AUTOCONFIGURE, BASE AND VECTOR ADDRESSES

A.1 OVERVIEW

The following discussion presents the algorithm for assignment of floating addresses and vectors for all DEC operating systems. Bus addresses are discussed in subsection 3.5.

A.2 DETERMINING THE CSR ADDRESS FOR USE WITH AUTOCONFIGURE

The term **autoconfigure** refers to a software utility that is run when the computer is bootstrapped. This utility finds and identifies I/O devices in the I/O page of system memory.

Some devices (such as the DM11) have fixed addresses reserved for them. Autoconfigure detects the presence of such a device simply by testing its standard address for a response. Specifically, the control and status register (CSR) address, which is usually the first register of the block, is tested.

Addresses for those devices not assigned fixed numbers are selected from the floating CSR address space (760010 - 763776) of the LSI-11 bus input/output (I/O) page. This means that the presence or absence of floating devices affects the assignment of addresses to other floating-address devices. Similarly, many devices have floating interrupt vector addresses. According to the DEC standard, vectors must be assigned in a specific sequence, and the presence of one type of device affects the correct assignment of vectors for other devices.

The base address for a floating-address device is selected according to the algorithm used during autoconfigure. The algorithm is used in conjunction with a device table (Table A-1).

Essentially, autoconfigure checks each valid base address in the floating LSI-11 bus address space for the presence of a device. Autoconfigure expects any devices installed in that space to be in the order specified by the device table. Also, the utility expects an eight-byte block to be reserved for each device that is not installed in the system. The presence of each empty block tells autoconfigure to look at the next valid address for the next device on the list.

When a device is detected, a block of addresses is reserved for the device according to the number of registers it employs. The utility then looks at the next base address for that device type. If there is a device there, it is assumed to be of the same type as the one before it, and a block is reserved for that device. If there is no

response at the next address, that space is reserved to indicate that there are no more devices of that type. Then the utility checks the base address (at the appropriate boundary) for the next device in the table.

Table A-1. SYSGEN Device Table

Rank	Device	Number of Registers	Octal Modulus	Rank	Device	Number of Registers	Octal Modulus
1	DJ11	4	10	17	Reserved	4	10
2	DH11	8	20	18	RX11[2]	4	10
3	DQ11	4	10	18	RX211[2]	4	10
4	DU11,DUV11	4	10	18	RXV11[2]	4	10
5	DUP11	4	10	18	RXV21[2]	4	10
6	LK11A	4	10	19	DR11-W	4	10
7	DMC11	4	10	20	DR11-B[3]	4	10
7	DMR11	4	10	21	DMP11	4	10
8	DZ11[1]	4	10	22	DPV11	4	10
8	DZV11	4	10	23	ISB11	4	10
8	DZS11	4	10	24	DMV11	8	20
8	DZ32	4	10	25	DEUNA[2]	4	10
9	KMC11	4	10	26	UDA50[2]	2	4
10	LPP11	4	10	27	DMF32	16	40
11	VMV21	4	10	28	KMS11	6	20
12	VMV31	8	20	29	VS100	8	20
13	DWR70	4	10	30	TU81	2	4
14	RL11[2]	4	10	31	KMV11	8	20
14	RLV11[2]	4	10	32	DHV11	8	20
15	LPA11-K[2]	8	20	33	DMZ32	16	40
16	KW11-C	4	10	34	CP132	16	40

[1] DZ11-E and DZ11-F are treated as two DZ11s.

[2] The first device of this type has a fixed address. Any extra devices have a floating address.

[3] The first two devices of this type have a fixed address. Any extra devices have a floating address.

In summary, there are four rules that pertain to the assignment of device addresses in floating address space:

1. Devices with floating addresses must be attached in the order in which they are listed in the Device Table, Table A-1.

2. The base address for a given device type is assigned on word boundaries according to the number of LSI-11 bus-accessible registers that the device has. The following table relates the number of device registers to possible word boundaries.

Device Registers	Possible Boundaries
1	Any Word
2	XXXXX0, XXXXX4
3,4	XXXXX0
5,6,7,8	XXXX00,XXXX20,XXXX40,XXXX60
9 through 16	XXXX00,XXXX40

The autoconfigure utility inspects for a given device type only at one of the possible boundaries for that device. That is, the utility does not look for a DMF32 (16 registers) at an address that ends in 20.

3. A gap must follow the register block of any installed device to indicate that there are no more of that type of device. This gap must start on the proper base address boundary for that type of device.

4. A gap must be reserved in floating address space for each device type that is not installed in the current system. The gap must start on the proper word boundary for the type of device the gap represents. That is, a single DJ11 installed at 760010 would be followed by a gap starting at 760020 to show a change of device types. A gap to show that there are none of the next device on the list (DH11) would begin at 760040, the next legal boundary for a DH11-type device.

A.3 DETERMINING THE VECTOR ADDRESS FOR USE WITH AUTOCONFIGURE

A floating vector address convention is used for communications and other devices that interface with the LSI-11 bus. These vector addresses are assigned in sequence, starting at 300 and proceeding upward to 777. Table A-2 shows the assignment sequence.

For a given system configuration, the device with the highest floating vector rank is assigned to vector address 300. Additional devices of the same type are assigned subsequent vector addresses according to the number of vectors required per device, and according to the starting boundary assigned to that device type.

Table A-2. Priority Ranking for Floating Vector Addresses (starting at 300 and proceeding upward)

Rank	Device	Number of Vectors	Octal Modulus
1	DC11	2	10
1	TU58	2	10
2	KL11[1]	2	10
2	DL11-A[1]	2	10
2	DL11-B[1]	2	10
2	DLV11-J[1]	8	40
2	DLV11,DLV11-F[1]	2	10
3	DP11	2	10
4	DM11-A	2	10
5	DN11	1	4
6	DM11-BB/BA	1	4
7	DH11 modem control	1	4
8	DR11-A, DRV11-B	2	10
9	DR11-C, DRV11	2	10
10	PA611 (reader+punch)	4	20
11	LPD11	2	10
12	DT07	2	10
13	DX11	2	10
14	DL11-C to DLV11-F	2	10
15	DJ11	2	10
16	DH11	2	10
17	VT40	4	20
17	VSV11	4	10
18	LPS11	6	40
19	DQ11	2	10
20	KW11-W, KWV11	2	10
21	DU11, DUV11	2	10
22	DUP11	2	10
23	DV11 + modem control	3	20
24	LK11-A	2	10
25	DWUN	2	10
26	DMC11	2	10
26	DMR11	2	10
27	DZ11/DZS11/DZV11	2	10
27	DZ32	2	10
28	KMC11	2	10
29	LPP11	2	10

(continued on next page)

Table A-2. Priority Ranking for Floating Vectors Addresses (starting at 300_8 and proceeding upward) (continued)

Rank	Device	Number of Vectors	Octal Modulus
30	VMV21	2	10
31	VMV31	2	10
32	VTV01	2	10
33	DWR70	2	10
34	RL11/RLV11[2]	1	4
35	**TS11[2], TU80[2]**	**1**	**4**
36	LPA11-K	2	10
37	IP11/IP300[2]	1	4
38	KW11-C	2	10
39	RX11[2]	1	4
39	RX211[2]	1	4
39	RXV11[2]	1	4
39	RXV21[2]	1	4
40	DR11-W	1	4
41	DR11-B[2]	1	4
42	DMP11	2	10
43	DPV11	2	10
44	ML11[3]	1	4
45	ISB11	2	10
46	DMV11	2	10
47	DEUNA[2]	1	4
48	UDA50[2]	1	4
49	DMF32	8	40
50	KMS11	3	20
51	PCL11-B	2	10
52	VS100	1	4
53	Reserved	1	4
54	KMV11	2	10
55	Reserved	2	10
56	IEX	2	10
57	DHV11	2	10
58	DMZ32	6	20
59	CP132	6	20

[1] A KL11 or DL11 used as a console, has a fixed vector.

[2] The first device of this type has a fixed vector. Any extra devices have a floating vector.

[3] ML11 is a MASSBUS device which can connect to a LSI-11 bus via a bus adapter.

Vector addresses are assigned on the boundaries indicated in the modulus column of Table A-2. That is, if the modulus is 10, then the first vector address for that device must end with zero (XX0). If the modulus is 4, then the first vector address can end with zero or 4 (XX0, XX4).

Vector addresses always fall on modulo 4 boundaries (XX0, XX4). That is, a vector address never ends in any number but 4 or 0. Consequently, if a device has two vectors and the first must start on a modulo 10 boundary, then, using 350 as a starting point, the vectors will be 350 and 354.

A.4 A SYSTEM CONFIGURATION EXAMPLE

Table A-3 presents an example of a system configuration that includes devices with fixed addresses and vectors, and floating addresses and/or vectors.

Table A-4 shows how the device addresses for the floating address devices in Table A-3 were computed, including gaps.

Table A-3. Base and Vector Address Example

Controller	Vector	Base Address
1 DN11	300	775200
1 DU11	310	760040
1 DV11	320	775000
1 DMC11	340	760100
2 DZ11s	350	760120
	360	760130
2 TS11s	224	772520
	370	772524
3 DR11Bs	124	772410
	400	772430
	410	760300

Table A-4. Floating Address Computation

Installed	Device	Address	Installed	Device	Address
	DJ11 Gap	760010		LPP11 Gap	760160
	DH11 Gap	760020		VMV21 Gap	760170
	DQ11 Gap	760030		VMV31 Gap	760200
--->	DU11	760040		DWR70 Gap	760210
	DU11 Gap	760050		RL11 Gap	760220
	DUP Gap	760060		LPA11 Gap	760230
	LK11 Gap	760070		KWC11 Gap	760240
--->	DMC11	760100		Reserved	760250
	DMC11 Gap	760110		RX211 Gap	760260
--->	DZ11	760120		DR11W Gap	760270
--->	DZ11	760130	--->	DR11B	760300
	DZ11 Gap	760140		DR11B Gap	760310
	KMC11 Gap	760150			

BLANK

Appendix B
PROM REMOVAL AND REPLACEMENT

B.1 OVERVIEW

This appendix provides instructions for PROM removal and replacement. PROMs are usually exchanged only when an emulation is to be changed or when necessary for maintenance. Owners of existing TC03 Tape Couplers may wish to take advantage of the flexibility of Emulex hardware by replacing their existing TS11 emulation PROM set with a PROM set for another compatible emulation at some future date. The PROM set consists of an emulation firmware set and the associated Address PROM.

This appendix is divided into three subsections, as listed in the following table:

Subsection	Title
B.1	Overview
B.2	Location
B.3	Removal and Replacement

B.2 LOCATION

The TC03 Tape Coupler has six IC sockets for insertion of PROMs that store instructions used by the on-board microprocessor to perform the TS11 emulation. These sockets are located along the left edge of the PCBA and are reference designated U1 (PROM0), U2 (PROM1), U39 (PROM2), U40 (PROM3), U92 (PROM4), and U93 (PROM5), as shown in Figure 4-2 and listed in Table B-1. The number on the top of each PROM IC is an Emulex part number (P/N) that identifies the unique program pattern of the PROM.

Three other IC sockets are provided for replaceable ICs:

- Socket U98 (tenth IC from right, second row from bottom) contains the Address Decode PROM.
- Socket U121 (seventh IC from right, bottom row) is used for the optional Extended (22-bit) Address option. This option requires a bit-slice AMD 2908 IC.
- Socket U91 (fist IC on right, third row from bottom) contains the auto increment PROM.

Table B-1. PROM Locations

Emulex PROM P/N	Socket	Reference Designator
A80	PROM0	U1
A81	PROM1	U2
A82	PROM2	U39
A83	PROM3	U40
A84	PROM4	U92
A85	PROM5	U93

B.3 REMOVAL AND REPLACEMENT

To remove any replaceable IC, pry each installed IC from its socket by using an IC puller or equivalent tool. When inserting PROMs in sockets, be sure that the ID numbers on top of the PROMs are in the same sequence as the PROM reference designation numbers on the PCBA beside each respective PROM socket. For example, the PROM with ID3 must be inserted in IC socket reference designated PROM3.

Verify that each PROM is seated firmly and that no pins are bent or misaligned. If the two rows of pins on any PROM are too far apart to fit in the IC socket, grasp the PROM at its ends between thumb and forefinger, press one row of pins on one side against a table top or other firm, flat surface, and gently bend the row of pins inward enough to allow the PROM to fit the intended IC socket.

Appendix C
DRIVE CONFIGURATION

C.1 OVERVIEW

The drive configuration tables in this appendix define the TC03 and drive switch settings for a variety of typical tape drives. Although not all vendors are covered, these tables can be used for configuring almost any vendor's drive:

Table	Title
C-1	TC03 Switch Settings for CDC 92181
C-2	CDC 92181 Jumper Placements and Switch Settings
C-3	TC03 Switch Settings for CDC 92185 and 92185-02
C-4	CDC 92185 Jumper Placements and Switch Settings
C-5	CDC 92185-02/04 Jumper Placements and Switch Settings
C-6	TC03 Switch Settings for Cipher 891
C-7	Cipher 891 Switch Settings
C-8	TC03 Switch Settings for Cipher 990
C-9	Cipher 990 Operating Parameter Values
C-10	TC03 Switch Settings for Kennedy 9400
C-11	Kennedy 9400 Switch Settings
C-12	TC03 Switch Settings for Kennedy 9X00F Series
C-13	Kennedy 9000F, 9100F, and 9300F Switch Settings

C.2 CDC 92181

The CDC 92181 is a 1600-bpi only, 25/100 ips streaming-type tape drive with its own embedded formatter. This transport supports all standard TS11 commands. It has several optional features and selectable addresses that must be considered during the installation process. Option and address selection components are contained on the Formatter/Control printed wiring assembly (PWA). Refer to the manufacturer's technical manual for component identification.

Tables C-1 and C-2 contain the recommended coupler and transport switch settings and jumper placements.

Table C-1. TC03 Switch Settings for CDC 92181

OPTION SWITCH	ON/OFF	NOTES
1-4	OFF	Drive should also be set for adaptive velocity control
2-9	ON	This will allow you to add a CDC 92185 on the daisy chain.
2-10	OFF	
3-9	OFF	
3-10	OFF	

Table C-2. CDC 92181 Jumper Placements and Switch Settings

Option	Component	Jumper or Switch Setting	Comments
Channel Parity Check	W1	1-2	As shipped; parity bit transferred with data.
Variable Short Gap (0.6 to 0.9 inch)	W3	1-2	
Fixed Long Gap (1.2 inches)	W4	2-3	As shipped.
Adaptive Velocity Control (AVC)	W5*	2-3	Enables auto speed select.
Formatter Address 0 (Transports 0-3)	S1 (at 21D)	OFF	As shipped.
Formatter Address 1 (Transports 4-7)	S1	ON	

Continued

Table C-2. CDC 92181 Jumper Placements and Switch Settings (Cont'd)

Option	Component	Jumper or Switch Setting	Comments
Transport Address 0, 4	S2 (at 21D) S3	OFF OFF	As shipped.
Transport Address 1, 5	S2 S3	OFF ON	
Transport Address 2, 6	S2 S3	ON OFF	
Transport Address 3, 7	S2 S3	ON ON	

* When this option is invoked, the transport enters a mode in which it selects the optimum speed to match system requirements: 25 ips streaming, 25 ips start/stop, or 100 ips mode. The choice of operating mode is automatic and does not require any involvement by the system. Thus the transport can be interfaced to a standard adapter and run under standard 0.5-inch tape software, and yet offer the advantage of streaming. With this option enabled, the unit responds normally to a Set 100 IPS command.

C.3 CDC 92185 AND 92185-02

The CDC 92185 series tape drive is a dual density drive that is capable of 1600 bpi and 6250 bpi operation. It operates at 25 ips in slow streaming mode and at 75 ips in high-speed streaming mode. It is available in two versions: unbuffered and buffered. The buffered version has an identification tag labeled "Buffered Std, I/O kit" on the inside lower right corner of the front door. The same TC03 tape coupler settings are used for both versions (Table C-3).

Option and address selection components are contained on the Interface, Formatter Write, and Servo/Control PWAs. Refer to the manufacturer's technical manual for component identification. Tables C-4 and C-5 summarize tape transport jumper placements and switch settings.

NOTE

The interface printed wiring assembly (PWA) is made from one of two printed wiring boards (PWBs): 77020320 or 77023050. Table C-4 lists the jumper and switch locations for both PWBs. To determine which PWB you have, check location G-6 on the interface PWA for the presence of W6. If W6 is present, the PWB is 77023050; if W6 is absent, the PWB is 77020320.

Table C-3. TC03 Switch Settings for CDC 92185 and 92185-02

OPTION SWITCH	ON/OFF	NOTES
SW 1-4	OFF	The transport should be set for adaptive velocity control
SW 2-9	ON	This allows use of old and new style formatter boards
SW 2-10	OFF	
SW 3-9	OFF	
SW 3-10	OFF	

Table C-4. CDC 92185 Jumper Placements and Switch Settings (Footnotes At End)

Option	Component	Jumper or Switch Setting	Comments
INTERFACE PWA (USING PWB 77020320)			
Channel Parity Check	W1	2-3	Parity enabled (as shipped).
Remote/Local Density	W3	OUT	Local density select (as shipped).
Adaptive Velocity Control (AVC)	W5	IN	AVC enabled.
Formatter/Device Address Select	S1	OFF	Formatter address 0, transports 0-3 (as shipped).
Formatter/Device Address Select	S1	ON	Formatter address 1, transports 4-7.
Formatter/Device Address Select	S2 S3	OFF OFF	Transport address 0 (FAD 0), 4 (FAD 1)
Formatter/Device Address Select	S2 S3	OFF ON	Transport address 1 (FAD 0), 5 (FAD 1)
Formatter/Device Address Select	S2 S3	ON OFF	Transport address 2 (FAD 0), 6 (FAD 1)
Formatter/Device Address Select	S2 S3	ON ON	Transport address 3 (FAD 0), 7 (FAD 1)
Not Used	S4	--	Not used.
INTERFACE PWA (USING PWS 77023050)			
Channel Parity Check	W1	2-3	Parity bit transferred with data from host (as shipped).
Remote/Local Density[1]	W3	2-3	Local density select (as shipped).
Adaptive Velocity Control (AVC)[2]	W5	1-2	AVC enabled (as shipped).

Continued

Table C-4. CDC 92185 Jumper Placements and Switch Settings (Continued)

Option	Component	Jumper or Switch Setting	Comments
Density Status Option	W6	2-3	Density status Disabled
Formatter/Device Address Select	S1	OFF	Formatter address 0, transports 0-3
Formatter/Device Address Select	S1	ON	Formatter address 1, transports 4-7
Formatter/Device Address Select	S2 S3	OFF OFF	Transport address 0 (FAD 0), 4 (FAD 1)
Formatter/Device Address Select	S2 S3	OFF ON	Transport address 1 (FAD 0), 5 (FAD 1)
Formatter/Device Address Select	S2 S3	ON OFF	Transport address 2 (FAD 0), 6 (FAD 1)
Formatter/Device Address Select	S2 S3	ON ON	Transport address 3 (FAD 0), 7 (FAD 1)
FORMATTER WRITE PWA (SERIES CODE 01 THROUGH 06)			
Long Gap Select (PE)	W1	1-2	Variable gap, 0.6 to 1.2 inches (as shipped)
Short Gap Select (PE)	W2	1-2	Variable gap, 0.6 to 0.9 in. (as shipped)
Long Gap Select (GCR)	W1	1-2	Variable gap, 0.3 to 0.6 in. (as shipped)
Short Gap Select (GCR)	W2	1-2	Variable gap, 0.3 to 0.45 in. (as shipped)
Spare	W3		Not used.

Continued

Table C-4. CDC 92185 Jumper Placements and Switch Settings (Continued)

Option	Component	Jumper or Switch Setting	Comments
FORMATTER WRITE PWA (SERIES CODE 07 AND ABOVE, OR EARLIER SERIES CODE WITH SPO 77026120)			
Gap Select	W1 W2	1-2 1-2	Variable short gap with I/O interface line FLGAP = FALSE (as shipped).
SERVO/CONTROL PWA			
Write to EEPROM	W1 W1	1-2 2-3	Active. Inactive.

1 If the transport is configured in the local density mode (W3, no jumper) and the tape is positioned at BOT, pressing the LOAD/REWIND switch repeatedly causes the unit to alternate between PE and GCR. The HIGH DENSITY indicator lights when GCR is selected.

2 When AVC is used, rather than selecting 25 ips mode when low speed is commanded, the transport enters a mode in which it chooses the optimum speed to match system requirements. This option allows the unit to be interfaced to a standard adapter and to run under standard 0.5-inch tape software, and yet to offer the advantage of streaming. With this option enabled, the unit responds to a SET 75 IPS command in the normal manner.

Table C-5. CDC 92185-02/04 Jumper Placements and Switch Settings

Option	Component	Jumper or Switch Setting	Comments
Enable Buffer	W4	1-2	Buffer operation enabled.
Enable AVC	W5	2-3	Enabled. AVC is operational only when the buffer is disabled.
Remote Density	W6	2-3	Enabled. Position for system density selection.
Error Recovery	W7	2-3	Disabled; automatic read error recover. (Write error recovery is always enabled.)
Ramp Delay	W10 W11 W12	0 (1-2) 0 (1-2) 0 (1-2)	Delay between command and data, 1 millisecond (msec)
Density Status	W13	2-3	Disabled. Interface status indicates PE always.
Write Parity	W14	2-3	Enabled. Checks Write Parity Line.
Interface Transfer Rate (F22)	S1 S2 S3	ON ON OFF	500K bytes/second
Maximum Block Size (F22)	S4 S5 S6	OFF ON ON	16K bytes
Formatter Address (H24)	S1 S1	OFF ON	Transport 0-3 Transport 4-7
Transport Address (H24)	S2 S3	OFF OFF	Address 0 (FAD 0), 4 (FAD 1)

Continued

Table C-5. CDC 92185-02/04 Jumper Placements and Switch Settings (Continued)

Option	Component	Jumper or Switch Setting	Comments
Transport Address (H24)	S2 S3	OFF ON	Address 1 (FAD 0), 5 (FAD 1)
Transport Address (H24)	S2 S3	ON OFF	Address 2 (FAD 0), 6 (FAD 1)
Transport Address (H24)	S2 S3	ON ON	Address 3 (FAD 0), 7 (FAD 1)

C.4 CIPHER 891

The Cipher 891 series tape drive is a data caching streamer that emulates start/stop operation. It is available in two versions: the 891-1 (1600 bpi, 100 ips) and the 891-2 (supports both 1600 and 3200 bpi at 100 ips). Table C-6 summarizes TC03 tape coupler switch settings for the Cipher 891, and Table C-7 lists tape transport signal line levels and option switch settings.

Table C-6. TC03 Switch Settings for Cipher 891

OPTION SWITCH	ON/OFF	NOTES
SW 1-4	ON	
SW 2-9	OFF	
SW 3-9	OFF	
SW 3-10	OFF	

Table C-7. Cipher 891 Switch Settings

Switch	Position 1	2	3	4	5	6	7	8	Function
U5W									Unit Address Select
	ON	ON	ON						FAD0 0
	ON	OFF	ON						1
	OFF	ON	ON						2
	OFF	OFF	ON						3
	ON	ON	OFF						FAD1 4
	ON	OFF	OFF						5
	OFF	ON	OFF						6
	OFF	OFF	OFF						7
				OFF					Post-EOT Streaming Enabled
					ON				3200 BPI Ident Disabled
U3T	OFF								EOT Location Disabled
		ON							External Parity
			OFF	OFF					Maximum Block Size 9K bytes
					ON				Disable Ramp Delay
						ON	ON	ON	Selected Simulated Speed, 250 (200-300) ips; Data Burst Transfer Rate 400K bytes/sec (320-480); Ramp Delay 1.0 msec.

C.5 CIPHER 990

The Cipher 990 is a start/stop emulating caching streamer. It features tri-density operation (1600, 3200, or 6250 bpi) at simulated tape speed of up to 100 ips at 1600 bpi.

We recommend that interconnection of Cipher's products and customer equipment be made with a harness of individual twisted pairs, each with the following characteristics:

- Maximum total cable length 30 feet
- Not less than one twist per inch
- 22- or 24-gauge conductor with minimum insulation thickness of 0.01 inch
- Maximum cable length between daisy-chain units, 5 feet
- No more than 15 feet of cable between the host I/O port and the first GCR Cache Tape
- Terminators provided at the receiving end only of each interface line in both the TC03 coupler and the last tape drive; intermediate tape drives must not have terminators

The ground side of each twisted pair must be grounded within a few inches of the interface circuit. The mating connector (3M Part No. 3415-00001 or equivalent) must be wired by the user. For twisted-pair cables, use connector Viking Part No. 3VT25/OG JHN12 or equivalent. For interface connectors and pin locations, see the drive manufacturer's technical manual.

Table C-8 lists TC03 tape coupler switch settings for the Cipher 990, and Table C-9 lists tape transport parameters to be entered via the drive operator's panel.

Table C-8. TC03 Switch Settings for Cipher 990

OPTION SWITCH	ON/OFF	NOTES
SW 1-4	ON	
SW 2-9	OFF	
SW 3-9	OFF	
SW 3-10	OFF	

Table C-9. Cipher 990 Operating Parameter Values

Parameter	Default Value	Recommended Setting
Serial Port Baud Rate	300	150
Host Supplied Parity	No	Yes
Echo Read Strobes on Writes	Yes	Yes
EOT Mode	Normal	Normal
Echo 1600 bpi ID Burst	Yes	Yes
Echo 3200 bpi ID Burst	No	No
Echo 6250 bpi ID Burst	Yes	Yes
Abort Active Writes on Overwrites	No	No
Interface Transfer Rate	158K bytes/sec	632.8K bytes/sec
Default Density at Power Up	1600 bpi	6250 bpi
Maximum Block Size	9K	16K
Interface Ramp Delay	3 msec	0 msec
Filemark Write Sync	Yes	No
Read Error Retrys	4	4
Write Error Retrys	16	16
Error Correction On	Yes	Yes
Unit Logical Address	0	0
Lock Out 3200 bpi Write Error	No	No
Remote Density Select Enabled	Yes	No
Factory Mode	No	No

C.6 KENNEDY 9400

The Kennedy 9400 is a tri-density, embedded formatter, start/stop tape drive. It operates at 75 ips in either 800 or 1600 bpi, and at 45 ips at 6250 bpi.

The drive has only one switch that can be set by the user; it is located on the interface board and should be set as shown in Table C-11. When SW 4 is set for remote dual density select, SW 5 and 6 determine which two of the three possible densities are selected via the signal IDEN. IDEN is asserted (1) when the software selects 1600 bpi and negated (0) when the software selects 800 bpi.

Up to four drives can be daisy-chained. The terminating resistor packs in IC locations 5, 10, and 11 must be removed from all but the last transport in the chain.

TC03 coupler switch settings are listed in Table C-10.

Table C-10. TC03 Switch Settings for Kennedy 9400

OPTION SWITCH	ON/OFF	NOTES
SW 1-4	ON	
SW 2-9	OFF	
SW 3-9	OFF	
SW 3-10	OFF	

Table C-11. Kennedy 9400 Switch Settings

OPTION SWITCH	ON/OFF	NOTES
SW 1	OFF	Formatter address switch.
SW 2,3	OFF	Transport address switches. Should be OFF on all transports with the front panel option. Transport address is determined via the front panel.
SW 4	OFF	Remote Dual Density. The transport must be in remote position via the front panel. Two of the three densities are selected based on the status of the signal IDEN and transport switches 5 and 6. Requires special software.
SW 4	ON	Remote Tri-Density Select. This option requires an extra control signal not available on present transports. Requires special software.
SW 5 SW 6	OFF OFF	IDEN = 0, PE; IDEN = 1, GCR.
SW 5 SW 6	ON OFF	IDEN = 0, NRZI; IDEN = 1, GCR.
SW 5 SW 6	OFF ON	IDEN = 0, NRZI; IDEN = 1, PE.
SW 7,8	OFF	Data rate 312K bytes/second.

C.7 KENNEDY 9000F, 9100F, AND 9300F

The Kennedy 9X00F series tape drives are dual-density, single-speed transports with an attached 9220 formatter. All models support both 800 and 1600 bpi operation. The 9000F is a tension arm 45 ips drive, whereas the 9100F and 9300F are vacuum column, 75 ips/125 ips drives.

The formatter can be used with tape transports operating and seven different speeds, ranging from 12.5 to 125 ips. In NRZI operation, each of the four addressable transports can operate at a different speed; in PE operation, only two different speeds can be used. Two DIP switches, K14 and N14, are used to match the formatter write

clock frequency to the speed of each of the four addressable transports (Table C-13). PE operation also requires switch settings to distinguish between the high and low speeds, and insertion of a header that includes the PLO components required for the different speeds. See the manufacturer's technical manual for the speed selection header configuration.

C.7.1 SWITCHES

Each of the two switch packages shown in Table C-13 is divided into two groups of four switches each: 1 through 4 and 5 through 8. Each group is assigned to one of the four addressable transports, as shown in the table. The three lower-order switches of each group (1-3 and 4-7) select the speed according to assigned binary values. Switches 4 and 8 of each package are used only in PE, to indicate whether the other three switches of the group select high or low PE speed: ON = high speed, OFF = low speed. For example, in a system that includes two tape transports with tape unit 0 operating at 125 ips and unit 1 operating at 25 ips, the switch settings on K14 (Table C-13) would be as follows:

	Speed			H/L	Speed			H/L
K14 Switch Number	1	2	3	4	5	6	7	8
Tape Unit 0 (125 ips)	ON	ON	ON	ON	X	X	X	X
Tape Unit 1 (25 ips)	X	X	X	X	OFF	ON	ON	OFF

C.7.2 INTERFACE CABLING REQUIREMENTS

The 9X00F formatter board is designed to accept two 50-conductor 3M type ribbon cables. An adapter board type 5304 is available to utilize 100-pin edge connectors cable configuration. If 100-pin twisted pair cable is used, all wires should be 24 AWG minimum with insulation thickness not less than 0.1 inch. Twist should not be less than one per inch, and cable length should not exceed 20 feet. If ribbon cable is used, each cable should not exceed 20 feet in length. Edge connectors are Kennedy PN 121-0162-002 for 50-conductor ribbon. The connector is Kennedy PN 121-0159-002 for 100-pin edge.

C.7.3 DAISY-CHAINING

Up to three additional transports can be daisy-chained to the formatter in the 9X00F master by using ribbon cables and appropriate adapters.

Model 9000 transports require a cable set PN 190-4999-001, one 190-4778-001 control adapter, and one 190-4779-001 data adapter. The 3860 data terminator and 3841 control terminator PCBAs should be removed from all but the last physical transport.

To daisy-chain Models 9700, 9800, 9100, or 9300, use one 190-4747-001 adapter for each unit and two 190-4999-NLL cables (N = number of transports, LL = total length in feet).

If one Model 9000 is mixed with 9100, 9300, 9700, or 9800 transports, it must be physically the last transport. Data and control terminators must be removed from all but the last physical transport. Maximum total cable length must not exceed 20 feet for any daisy-chaining configuration. The transport address may be assigned by switches, located as follows:

- On the transport control masterboard for Model 9000
- On the 4747 adapter board for other than Model 9000
- Thumbwheel address switch, if ordered with the transport

Table C-12. TC03 Switch Settings for Kennedy 9X00F Series

OPTION SWITCH	ON/OFF	NOTES
SW 1-4	ON	
SW 2-9	OFF	
SW 3-9	ON	Inhibits On-the-Fly operations.
SW 3-10	ON	Uses the leading edge of the Write Strobe, as required by the 9220 formatter.

Table C-13. Kennedy 9000F, 9100F, and 9300F Switch Settings

	K14/N14 Switch Settings					
Speed (ips)	SW1*	SW2	SW3	SW5	SW6	SW7
12.5 (1**)	ON	OFF	OFF	OFF	OFF	ON
18.75 (2)	OFF	ON	OFF	OFF	ON	OFF
25 (3)	ON	ON	OFF	OFF	ON	ON
37.5 (4)	OFF	OFF	ON	ON	OFF	OFF
45 (5)	ON	OFF	ON	ON	OFF	ON
75 (6)	OFF	ON	ON	ON	ON	OFF
125 (7)	ON	ON	ON	ON	ON	ON

* Note that switch numbers appear upside down as viewed on a mounted formatter.

** Numbers in parentheses are binary values.

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